ANALOG ELECTRONIC CIRCUITS (AEC)

LABORATORY MANUAL

B.TECH (EE) : III– SEMESTER

PREPARED BY

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DEPARTMENT OF ELECTRICAL ENGINEERING

Signature of HOD: **Signature of lab incharge:**

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Vision of the Department:

To provide holistic education to build competent and productive researchers and graduates.

Mission of the Department:

M1: To provide quality education facilities for preparing professionals who match globalstandards.

M2: To create good atmosphere for research and innovation by providing state of the artlaboratories.

M3: To prepare a cadre of engineers and scientists who will cater to the industrialdevelopment and economic growth of the society and country in future.

M4: To strengthen industry- institute interactions and interactions with alumni for mutualbenefits by the exchange of knowledge, ideas and visions to promote lifelong learning.

Program Outcomes (PO's): -

PO1: **Engineering knowledge:** Apply the knowledge of basic sciences and fundamental engineering concepts in solving engineering problems.

PO2: **Problem analysis:** Identify and define engineering problems, conduct experiments and investigate to analyze and interpret data to arrive at substantial conclusions.

PO3: **Design/development of solutions:** Propose an appropriate solution for engineering problems complying with functional constraints such as economic, environmental, societal, ethical, safety and sustainability.

PO4: **Conduct investigations of complex problems:** Perform investigations, design and conduct experiments, analyze and interpret the results to provide valid conclusions.

PO5: **Modern tool usage:** Select/ develop and apply appropriate techniques and IT tools for the design and analysis of the systems.

PO6: **The engineer and society:** Give reasoning and assess societal, health, legal and cultural issues with competency in professional engineering practice.

PO7: **Environment and sustainability:** Demonstrate professional skills and contextual reasoning to assess environmental/ societal issues for sustainable development.

PO8: **Ethics:** An ability to apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work:** Function effectively as an individual and as a member or leader in diverse teams and in multi-disciplinary situations.

PO10: **Communication:** An ability to communicate effectively.

PO11: **Project management and finance:** Demonstrate apply engineering and management principles in their own / team projects in multi-disciplinary environment.

PO12: **Life-long learning:** An ability to do the needs of current technological trends at electrical industry by bridging the gap between academic and industry.

Program Specific Outcomes (PSO's): -

PSO1: Apply the knowledge of electrical engineering to analyze and solve the complex problems in electrical power and engineering with social utility.

PSO2: The application of recent techniques along with modern software tools for design, simulation and analyzing electrical systems.

PSO3: Adapting to technological changes and professional and societal needs by engaging in lifelong learning, thereby contributing to career development.

Program Educational Objectives (PEO's): -

PEO1: To apply fundamental knowledge in mathematics, science and engineering concepts in electrical engineering for the development of engineering field.

PEO2: To analyze, plan and design electrical system including modern methodologies to address the issues in a technically sound and economically viable manner.

PEO3: To develop a skillful workforce who can practice as a team professionally and ethically in a wide range of electrical engineering related fields.

PEO4: To prepare them for lifelong learning for successful carrier development by giving them the state- of the-art technology in the learning process.

Course Objectives: -

The laboratory enables students to get practical experience in design, realization and verification of

- Biasing circuit for MOSFET& BJT
- BJT common emitter circuit
- MOSFET common source circuit
- op-amp circuit as adder, differentiator, integrator, subtractor
- Design of differential amplifier circuit
- Study of oscillator circuit
- Study of power amplifier circuit

Course Outcomes: -

After successful completion of this course, the students will be able to demonstrate theability to –

- Acquire a basic knowledge in solid state electronics including diodes, MOSFET, BJT and operational amplifier.
- Develop the ability to analyze and design analog electronics circuits using discrete components.
- Observe the amplitude and frequency responses of common emitter circuits.
- Design , construct and take measurement of various analog circuits to compare experimental results in the laboratory with theoretical analysis.

Syllabus

3rd Semester	REE3C202	Analogue Electronics Lab	L-T-P 0-0-3	2 CREDITS

ANALOG ELECTRONIC CIRCUITS (AEC) – LAB

B.Tech (EE) : III - SEMESTER

LIST OF EXPERIMENTS :

Experiment No.	List of Experiment	Date of Experiment	Date of Submission	Mark	Remark
01	Design and simulate BJT bias circuit and compare the results.				
02	Design and simulate JFET/MOSFET bias circuit and compare the results.				
03	Design and simulate BJT common Emitter circuit and compare DC & AC performance.				
04	Design and simulate JFET/MOSFET common Emitter circuit and compare DC & AC performance.				
05	Determining the frequency response of a common Emitter Amplifier: low frequency, high frequency & mid frequency response and compare with simulated results.				

06	Differential amplifier circuit without & with current sources.				
07	Study of Darlington connections and current mirror circuits.				
08	Op-Amp frequency responses and compensation.				
09	Application of Op-Amp as differentiator,integrator square wave generator.				
10	Obtain the bandwidth of FET /BJT using square wave testing of an amplifier				
11	RC phase shift oscillator / wein bridge oscillator using Op-Amp/Crystal Oscillator.				
12	Study of Class -A & Class-B power amplifiers.				

DO'SANDDON'TS

DO'S:-

1. **Proper dress has to be maintained while entering in the Lab.**
2. **All students should come to the Lab with necessary tools.**
3. **Students should carry observation notes and record completed in all aspects.**
4. **Correct specifications of the equipment have to be mentioned in the circuit diagram.**
5. **Student should be aware of operating equipment.**
6. **Students should be at their concerned experiment table, unnecessary moment is restricted.**
7. **Student should follow the indent procedure to receive and deposit the equipment from the Lab Store Room.**
8. **After completing the connections Students should verify the circuits by the Lab Instructor.**
9. **The reading must be shown to the Lecturer In-Charge for verification.**
10. **Students must ensure that all switches are in the OFF position, all the connections are removed.**
11. **All patch cords and stools should be placed at their original positions.**

DON'Ts:-

1. Don't come late to the Lab.

2. Don't enter into the Lab with Golden rings, bracelets and bangles.

3. Don't make or remove the connections with power ON.

4. Don't switch ON the supply without verifying by the Staff Member.

5. Don't switch OFF the machine with load.

6. Don't leave the lab

Essential Electronics Laboratory Equipment

Setting up an electronics laboratory requires just a few essential pieces of equipment and tools. While specialty pieces of equipment may be essential for your application, the essential pieces of equipment are the same for nearly any electronics lab.

Multimeter

A multimeter's measurement flexibility combined with their precision and accuracy make multimeters an essential tool in any electronics lab. Multimeters will typically be able to measure both AC and DC voltage and current as well as resistance. Multimeters are often used in troubleshooting designs and testing prototype circuits. Multimeter accessories include transistor testing modules, temperature sensorprobes, high voltage probes, and probe kits. Multimeters are available for as little as $10 and can run several thousand for a high accuracy, high precision bench top unit.

Oscilloscope

Electronics are all about the signals and the oscilloscope is the primary measurement tool to observe the shape of signals. Oscilloscopes, often called oscopes or just scopes, display signals in a graphical format on a pair of axis, generally with Y as the voltage and X as the time. This is a very powerful way to quickly see the shape of a signal, determine what is going on in an electronic circuit and monitor performance or track down problems. Oscilloscopes are available in digital and analog variants, starting at a few hundred dollars and running in to the tens of thousands for the top of the line models. Digital scopes have several measurement and trigger options built in to the system which make measurement of peak-to-peak voltage, frequency, pulse width, rise time, signal comparisons, and recording waveforms simple tasks.

Soldering Iron

The core tool for assembling electronics is the soldering iron, a hand tool used to melt solder to form an electrical and physical connection between two surfaces. Soldering irons come in a few forms, with the cheapest being plugged directly in to an outlet from the hand tool. While these soldering irons work, for most electronics work a temperature controlled soldering station is much preferred. The tip of a soldering iron is heated by a resistive heater and often monitored by a temperature sensor to keep the temperature of the tip steady. Soldering iron tips are often removable and are available in a range of shapes and styles to accommodate different types of soldering work.

Precision Mechanical Tools

Every electronics labs need a few key mechanical hand tools to help with the basic tasks and make the more complex tasks much easier. Some of the key tools include shear cutters, wire strippers, ESD-safe tweezers, needle nose pliers, precision screw driver set, "third hand" tools, and alligator/test clips and leads. Some tools, such as the ESD safe tweezers, are essential for surface mount work while other tools, such as the "third hand" tool are very useful when soldering components to a PCB and the component, PCB, soldering iron and solder all need to be held in place.

Power Supply

In the end, it's difficult to test a circuit without applying power to it. Several types of power supplies are available to support electronics design and testing with a number of features. For a general purpose laboratory power supply, variable voltage and current controls are one of the most important features. This allows one supply to provide a wide range of voltages that can be adjusted for any application. Often these power supplies can operate in either a constant voltage or constant current mode, allowing rapid testing of components or portions of a design without building a specific power regulation circuit.

Other Equipment

The equipment above only scratches the surface of the equipment that is available and might be critical for your application. Some of the other common equipment with more of a focused use includes:

- Function Generators
- Signal Generators
- Transistor Tester

Experiment No. 1

Design and simulate BJT bias circuit and compare the results.

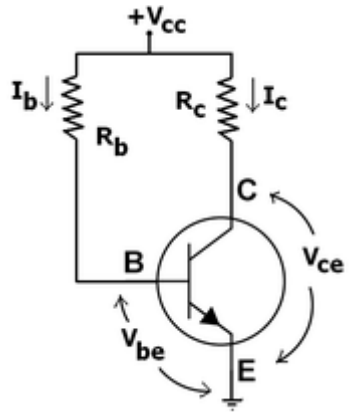
(1.a)Aim Of The Experiment:-

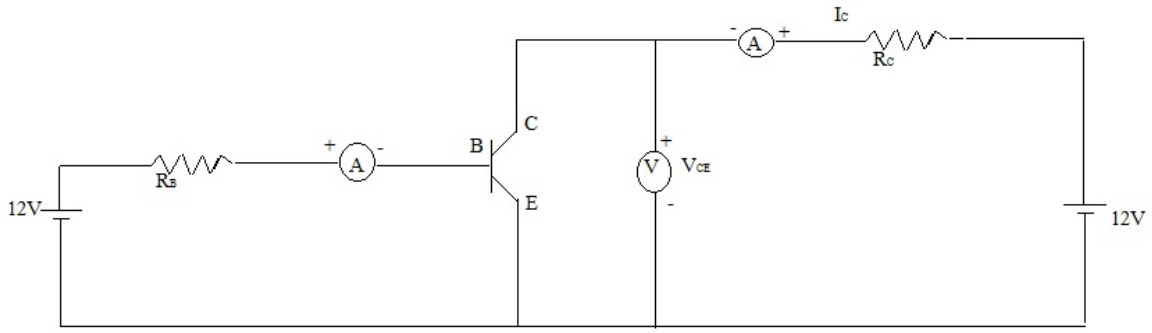
To study about the base bias circuit operation and analysis.

Equipments Needed:

Sl. No	Name of Apparatus	Specification	Quantity
1	BJT Biasing Trainer		
2	Ammeters		
3	voltmeters		
4	Patchchords		

Circuit Diagram:





THEORY:-

BASE BIAS-

Circuit Operation & Analysis:-

The transistor bias arrangement shown in below fig-1 is known as BASE BIAS & also known as fixed current bias. The base current is a constant quantity determined by supply voltage V_{CC}& base resistor R_B. Because V_{CC} & R_B are constant quantities, I_B remain fixed at a particular level. Unlike some other bias circuits, the base current is base bias circuit is notaffected by the transistor current gain.

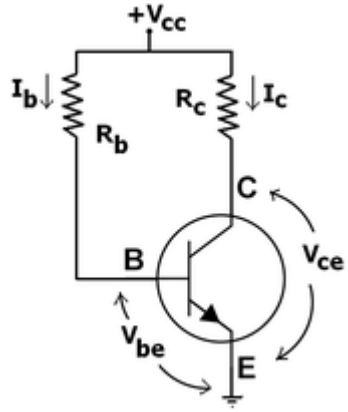


Figure1

From Fig-1 ,the voltage drop across R_B is ($V_{CC} – V_{BE}$) , and the base current is,

$\mathbf{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$

The base emitter voltage(V_{BE}) is taken as 0.7v for a Si transistor , & as 0.3V for a Ge device.

The transistor collector current is calculated as ,$\mathbf{I_C = h_{fe} * I_B}$.

The collector current is now used with ($V_{CE} = V_{CC} – I_C R_C$) to calculate the collector-emitter voltage. Thus, when the supply voltage and component values are known, a base bias circuit is easily analysed to determine the circuit current and voltages levels.

DESIGN PROCEDURE:

i) The base bias circuit is shown in the above figure(1) has R_S = 140 KΩ , R_C = 200Ω ,V_{CC}=12V & transistor has h_{fE}= 246. Determine I_B ,I_C and V_{CE}.

$\mathbf{I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{140K\Omega} = 81\mu A}$

$\mathbf{I_C = h_{fE} I_B} = 246 \times 81_{\mu A}$

$\mathbf{= 20mA}$

$\mathbf{V_{CE} = 8V}$

ii) By using variable potentiometers keep R_B= 140KΩ , R_C = 200 Ω.

iii) By using connecting wires connect the circuit as shown .

iv) Measure base current(I_B) and collector current I_C and collector to emitter voltage(V_{CE}).

v) Verify theoretical value and practical value.

Note:

We can also design base bias circuit for values of R_B and R_C calculateI_B ,I_C,V_{CE}& verify values.

OBSERVATION TABLE

SL NO.	I_B	I_C	V_{CE}	Theoretical Values	Practical Values

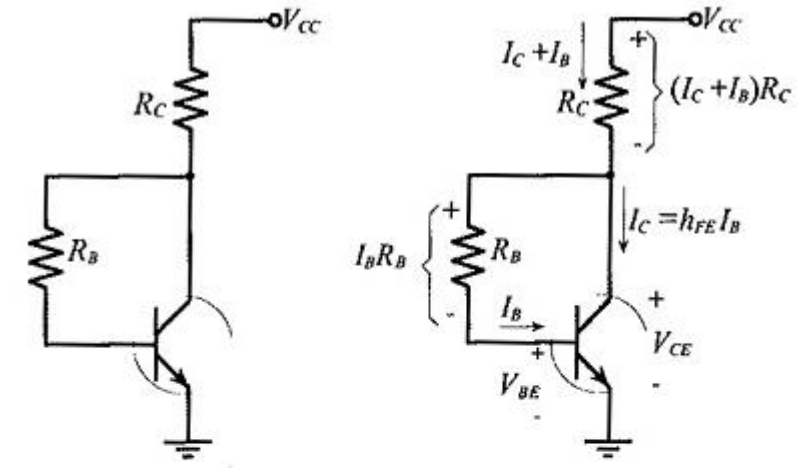
OBJECTIVE:

(1.b) To study about the collector to base bias circuit operation and analysis.

APPARATUS REQUIRED:-

Sl. No	Name of Apparatus	Specification	Quantity
1	BJT Biasing Trainer		
2	Ammeters		
3	Voltmeters		

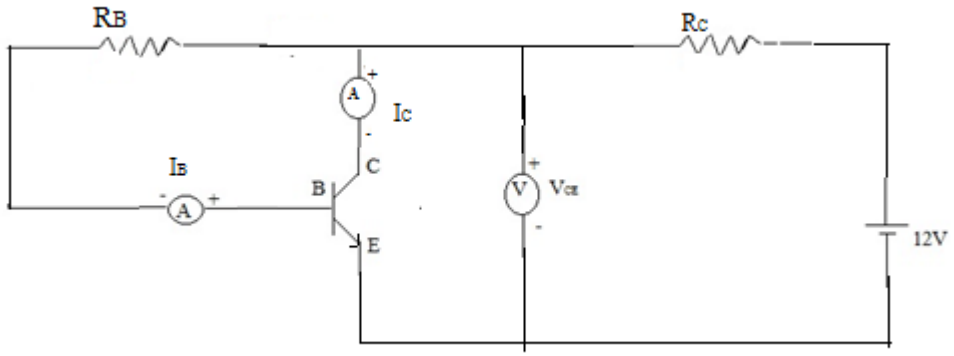
Circuit Diagram:



(a) Collector-to-base bias circuit

(b) Circuit currents and voltage drops

Figure
Collector-to-base bias circuits. Any change in V_{CE} changes I_B. The I_B change causes I_C to change, and this tends to return V_{CE} toward its original level.



THEORY:-

COLLECTOR-BASE BIAS-

Circuit Operation & Analysis:-

The collector to base circuit shown below has the base resistor(R_g) connected between the transistor collector and base terminals.As will be demonstrated,this circuit has significantly improved bias stability for h_{fe} changes compared to base bias.

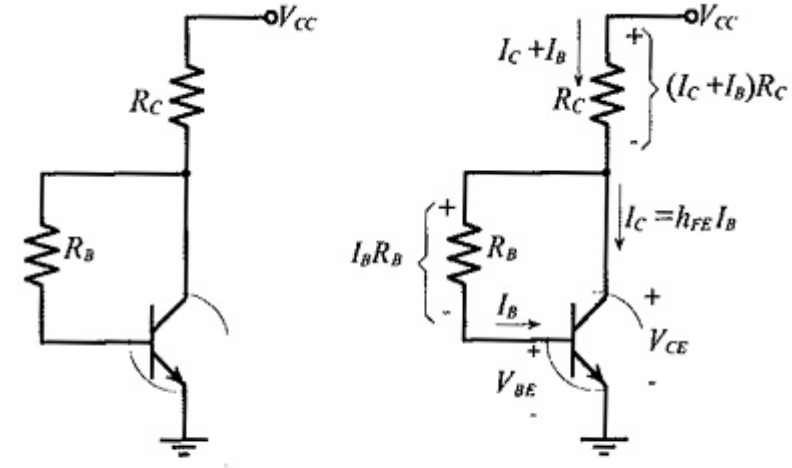
Refer to fig. note the voltage across R_B is dependent on $V_{CE.}$

$V_{CE} = V_{BE} + I_BR_B$

$I_b=\frac{V_{CC}-V_{BE}}{R_B}$

giving ,

$V_{CE} = V_{CC} – R_c(I_C + I_B)$



(a) Collector-to-base bias circuit

(b) Circuit currents and voltage drops

If I_C increases above the design level , there is an increase voltage drop across R_C, resulting in a reduction in V_{CE}. The reduced V_{CE} level causes I_B to be lower than its design level, and because $I_C = h_{fE}I_B$,the collector current is also reduced.Thus ,an incrase in I_C produces a feedback effect that tends to return I_C toward its original level. Similarly, a reduction in I_C produces an incrase in V_{CE} which increases I_B , thus tending to incrase I_C back to its original level.

Analysis of this circuit is a little more complicated than base bias analysis. To simplify the process, an equation is first derive for the base current.

$\mathbf{V_{BE} + I_BR_B = V_{CC} – R_c(I_C + I_B)}$

Substituting $\mathbf{I_C = h_{fE} I_B}$ into the above equation.

This gives ,

$\mathbf{V_{BE} + I_BR_B = V_{CC} – R_c(h_{fE} I_B + I_B)}$

$$\mathbf{I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(h_{fE} + 1)}}$$

OBSERVATION TABLE

SL NO.	I_B	I_C	V_{CE}	Theoretical Values	Practical Values

DESIGN PROCEDURE:

i) The collector to base bias circuit is shown in the above figure(1) has R_B =215KΩ , R_C = 1.39 KΩ , V_{CC} = 12V and the transistor h_{fE}= 246.

Determine I_B , I_C and V_{CE} .

$$\mathbf{I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(h_{fE} + 1)}} = \frac{12 - 0.7}{215 + 1.39(246 - 1)} = 20\mu A$$

$\mathbf{I_C = h_{FE} \times I_B}$ = 246 × 20µA = 4.92 mA

$V_{CE} = V_{CC} – R_C (I_C + I_B)$

= 12V- 1.39Kµ (4.92 ma + 20 µA)

V_{CE} = 5.13V

ii) By using variable potentiometers keep R_B=215KΩ , R_C= 1.39 KΩ .

iii) By using connecting wires connect the circuit as shown in the fig 1.

iv) Measure Base current

v) (I_B) & collector current (I_C) & collector to emitter voltage V_{CE}.

vi) Verify the theoretical & practical values.

OBSERVATION TABLE

SL NO.	I_B	I_C	V_{CE}	Theoretical Values	Practical Values

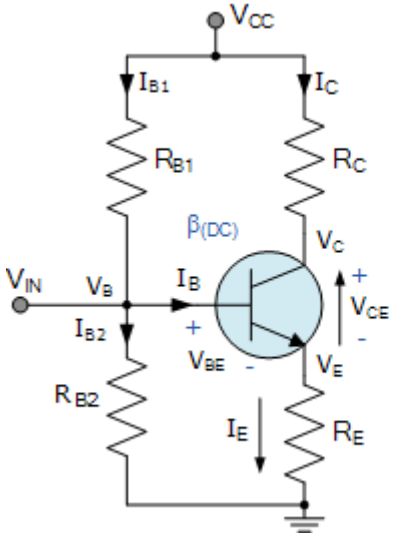
OBJECTIVE:

(1.c) To Study about the voltage divider bias circuit operation and analysis.

APPARATUS REQUIRED:-

Sl. No	Name of Apparatus	Specification	Quantity
1	BJT Biasing Trainer.		
2	Ammeters.		
3	Voltmeters		
4	Patch chords.		

Circuit Diagram:



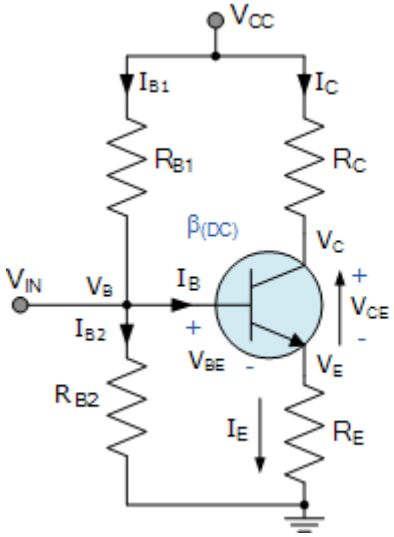
$$V_C = V_{CC} - R_C I_C = (V_E + V_{CE})$$
$$V_E = I_E R_E = V_B - V_{BE}$$
$$V_{CE} = V_C - V_E = V_{CC} - (I_C R_C + I_E R_E)$$
$$V_B = V_{BE} + V_E = V_{RB2} = \left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right) V_{CC}$$
$$I_{B2} = \frac{V_B}{R_{B2}}$$
$$I_{B1} = I_B + I_{B2} = \frac{V_{CC} - V_B}{R_{B1}}$$
$$R_B = \frac{R_{B1} \times R_{B2}}{R_{B1}+R_{B2}} \qquad I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta)R_E}$$
$$I_C = \beta_{(DC)} I_B$$
$$I_E = I_C + I_B = \frac{V_E}{R_E}$$

THEORY:-

VOLTAGE DIVIDER BIAS-

Circuit Operation & Analysis:-

Voltage divider bias, also known as emitter current bias , is the most stable of the three basic transistor bias circuits.The **voltage divider bias** figure is as shown below.



$$V_C = V_{CC} - R_C I_C = (V_E + V_{CE})$$
$$V_E = I_E R_E = V_B - V_{BE}$$
$$V_{CE} = V_C - V_E = V_{CC} - (I_C R_C + I_E R_E)$$
$$V_B = V_{BE} + V_E = V_{RB2} = \left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right) V_{CC}$$
$$I_{B2} = \frac{V_B}{R_{B2}}$$
$$I_{B1} = I_B + I_{B2} = \frac{V_{CC} - V_B}{R_{B1}}$$
$$R_B = \frac{R_{B1} \times R_{B2}}{R_{B1}+R_{B2}} \qquad I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta)R_E}$$
$$I_C = \beta_{(DC)} I_B$$
$$I_E = I_C + I_B = \frac{V_E}{R_E}$$

The collector (R_C) , there is an emitter resistor (R_E) connected in series with the transistor. The total dc load in series with the transistor is (R_C + R_E), and this total resistance must be used when drawing the DC load line for the circuit. Resistors R_1 and R_2 constitute a voltage divider the supply voltage to produce the base bias voltage (V_B).Voltage divider bias circuits are normally designed to have the voltage divider current(I_2) very much larger than the transistor base current(I_B). In this circumstance, V_B is largely unaffected by I_B .So, V_B can be assumed to remain constant.

Referring to Fig. 3(b),

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

With $V_B$constant , the voltage across the emitter resistor is also a constant quantity.,

$V_E = V_B - V_{BE}$

This means that the emitter current is constant.

The collector current is approximately equal to the emitter current. So, I_C is held at a constant level.

Again referring to fig.3(b) , the transistor collector voltage is

$\mathbf{V_C = V_{CC} - (I_C R_C)}$

$\mathbf{I_E = \frac{V_B - V_{BE}}{R_E}}$

The collector-emitter voltage is

$\mathbf{V_{CE} = V_C - V_E}$

$\mathbf{V_{CE}}$ can also be determined as,

$\mathbf{V_{CE} = V_{CC} - I_C(R_C + R_E)}$

Clearly, with I_C and $I_E$constant , the transistor collector-emitter voltage remains at a constant level.

DESIGN PROCEDURE:

I. **T**he voltage divider bias is shown in the above fig has R_1 =33KΩ ,R_2 =12KΩ , R_C =1.2KΩ ,R_E =1KΩ ,V_{CC} = 12V and the transistor has h_{FE} = 246 . Determine I_B ,I_C , and V_{CE}.

$$\mathbf{I_B = \frac{V_T - V_{BE}}{R_T + R_E(h_{fE} + 1)}}$$

$$\mathbf{V_T = \frac{V_{CC} \times R_2}{R_1 + R_2} = \frac{12 \times 12K\Omega}{33K\Omega + 12K\Omega} = 3.2K\Omega}$$

$$\mathbf{R_T = \frac{R_1}{R_2} = \frac{33K\Omega}{12K\Omega} = 8.8\ K\Omega}$$

$$\mathbf{I_B = \frac{3.2 - 0.7}{8.8K\Omega + 1K\Omega(246 + 1)} = 9.7\mu A}$$

$\mathbf{I_C = h_{fE} \times I_B} = 246 \times \mathbf{9.7\mu A = 2.38mA}$

$\mathbf{I_E = I_B + I_C = 9.7\mu A + 2.38mA = 2.38mA}$

$\mathbf{V_E = I_E R_E = 2.38mA \times 1}K\Omega = 2.38V$

$\mathbf{V_C = V_{CC} - I_C R_C = 12 - (2.38mA \times 1.2\ K\Omega) = 12 - 2.85 = 9.15}$

$\mathbf{V_{CE} = V_C - V_E} = 9.15 - 2.38 = 6.77V$

II. By using variable potentiometers, keep R_1 = 33**KΩ ,** R_2 = 1.2**KΩ ,** R_C = 1.2**KΩ ,** R_E = 1**KΩ**

III. By using connecting wires connect the circuit is shown in the fig.

IV. Measure base current (I_B) and collector current (I_C) and collector to emitter voltage V_{CE} .

V. Verify the theoretical and practical values.

OBSERVATION TABLE

SL NO.	I_B	I_C	V_{CE}	Theoretical Values	Practical Values

RESULT:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

Viva Question

1. What do you mean by transistor biasing? What is its need?

2. What do you understand by stabilization of operating point?

3. Mention the essential of biasing circuit?

4. Describe various methods used for transistor biasing. State their advantages and disadvantages?

Experiment NO. 2

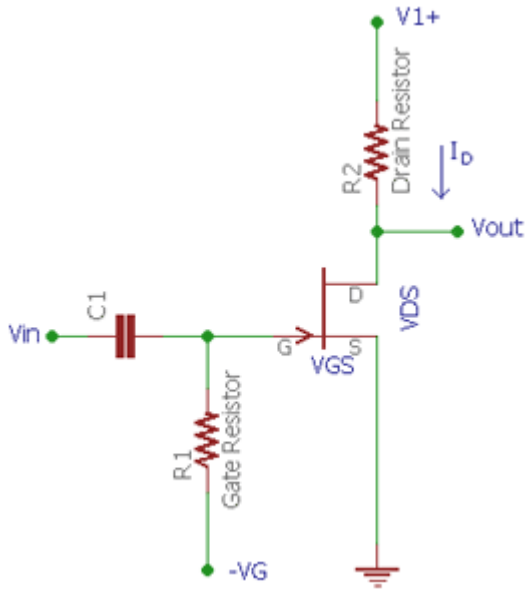
Design and simulate JFET/MOSFET bias circuit and compare the results.

Aim Of The Experiment:

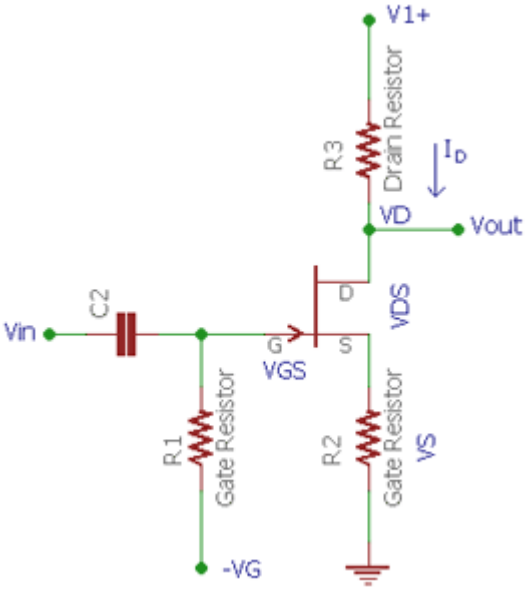
Design and simulate JFET/MOSFET bias circuit and compare the results.

Sl. No	Name of Apparatus	Specification	Quantity
1	JFET amplifier kit		
2	Patch chords& probe		
3	CRO		
4	Multimeter		

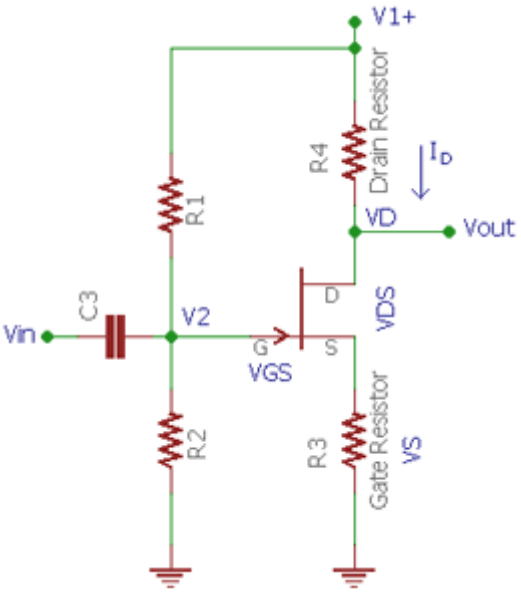
Circuit Diagram:- (a)Fixed bias circuit:



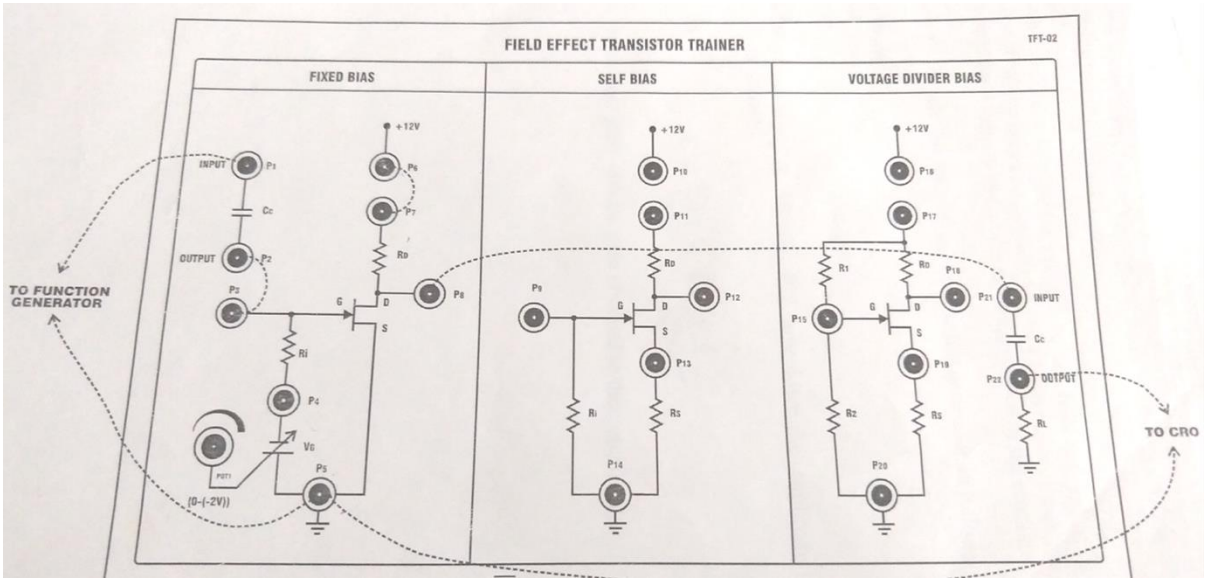
(b)SELF BIAS CIRCUIT:



(C)VOLTAGE DIVIDER BIAS CIRCUIT:



Connection diagram:

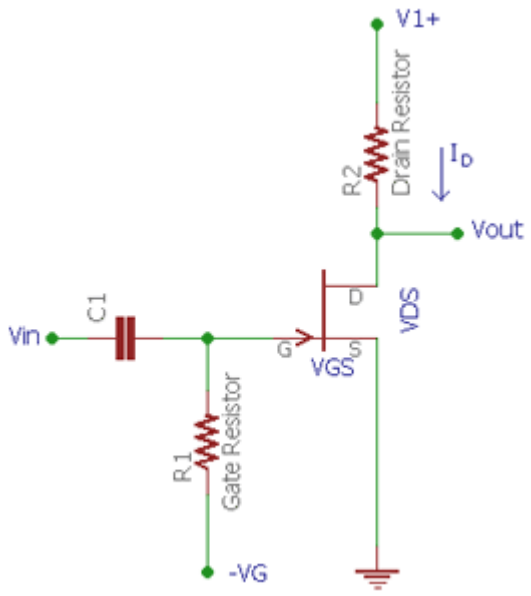


Theory:-

FET is a square law device, the relationship between i/p & o/p characteristics are nonlinear.

FIXED BIAS:-

It is also named as a gate bias since negative voltage feed to the gate terminal of the JFET. The resistor $R_g$is present to ensure that the input acsignal appears at the input to the FET amplifier for the ac analysis. If the gate is directly connected to the bias source(instead of using R_g) , any ac signal applied to the gate would be short circuited to V_g .There is no gate current to produce voltage drop across R_g. So the gate-source voltage remains constant at V_g.

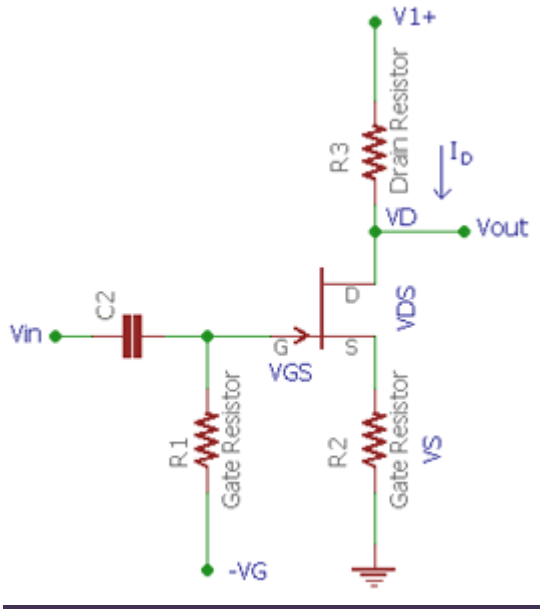


The gain of the biasing circuit depends on the drain current of the FET , the drain current depends on the gate – source voltage of the FET. So the gain of the circuit can be set by suitably setting the gate – source voltage. The drain current can also be set by drain – source voltage which depends on the drain resistor $R_{d.}$ So the ac voltage gain of the circuit can be determined by the drain resistor. The gain of the circuit limits to the particular higher value of the drain resistance, after these value the drain current falls which reduces the gain of the gain of the circuit. The coupling capacitors are “open circuits” for the DC analysis & low impedances(essentially short circuits) for the AC analysis.

SELF BIAS CIRCUIT:

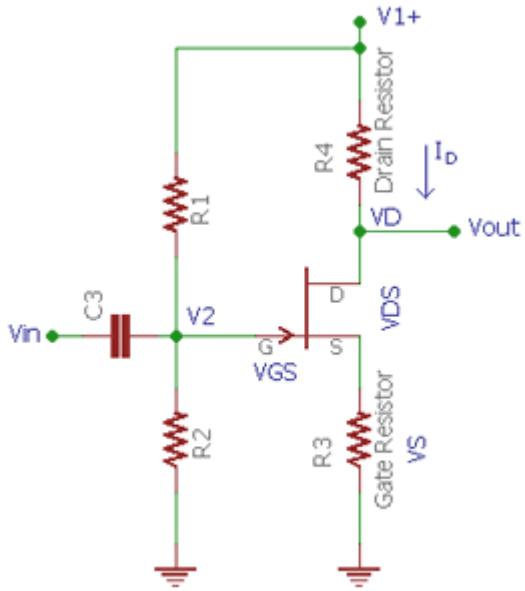
In self-biasing technique, a single resistor is added across the source pin. The voltage drop across the source resistor R2 creates the V_{GS} to bias the voltage. In this technique, the gate current is zero again. The source voltage is determined by the same ohms law V = I x R. Therefore source voltage = Drain current x source resistor. Now, the gate to source voltage can be determined by the differences between gate voltage and source voltage.

Since the gate voltage is 0 (as the gate current flow is 0, as per V = IR, gate voltage = Gate current x gate resistor = 0) the V_{GS} = 0 – Gate current x Source resistance. Thus there is no external biasing source is needed. The biasing is created by self, using the voltage drop across source resistor.



Voltage Divider Bias:-

In self bias circuit, increasing the value of source resistance will increase the drain current to maximum level. If we increases the source resistance further then the drain current will falls down. This limits the selection of source resistance. This limitation can be reduced by using voltage divider bias. Here the gate bias can be derived from supply voltage by means of voltage divider resistors R1 & R2. The gate voltage does not goes to negative value at any time, gate – source voltage calculated by taking difference between gate voltage & source voltage.



The difference between the self bias circuit & voltage divider is only the inclusion of one bias resistor R1 which will biases the gate terminal of the FET. The variation in drain- source

voltage is very large value for fixed bias and it will be decreased in voltage divider bias & it will more suitable for commercial use.

Procedure:

fixed bias:-

1. Make wiring connections for small signal fixed bias circuit as per wiring diagram which is provided at the end of this experiment.
2. Ensure that the trainer is switched off &donot feed any signal at test point P3.
3. Connect a multimeter between test points P3 & P4 to measure input resistance.Note down the resistance value which is the input impedance of the circuit.
4. Switch ON the trainer , set the setting on Function Generator as follows.
   Function mode – Sine
   Signal frequency – 1 KHz
   Amplitude – 250 mV
5. Observe the output signal at the test point P22 , Note down the amplitude level. Calculate voltage gain as follows.
   $\mathbf{A_V = \frac{V_{Out}}{V_{in}}}$
6. Compare the voltage gain with gain obtained in theoretical value.

Self biases circuit:-

1. Make wiring connections for small signal self biases circuit as per wiring diagram which is provided at the end of this experiment.
2. Ensure that the trainer is switched off & donot feed any signal at test point P9.
3. Connect a multimeter between test points P9& P14 to measure input resistance.Note down the resistance value which is the input impedance of the circuit.
4. Switch ON the trainer , set the setting on Function Generator as follows.
   Function mode – Sine
   Signal frequency – 1 KHz
   Amplitude – 250 mV
5. Observe the output signal at the test point P22 , Note down the amplitude level. Calculate voltage gain as follows.
   $\mathbf{A_V = \frac{V_{Out}}{V_{in}}}$
6. Compare the voltage gain with gain obtained in theoretical value.
7. Source Voltage, $V_S = I_D R_S$
   $$V_S = 1.7\times 10^{-3} \times 1 \times 10^{3}$$
   $$= 1.7\ V$$
8. Drain to Source voltage , $V_{DS} = V_{DD} - I_D(R_D + R_S)$
   $$V_{DS} = 12 - 1.7\times 10^{-3}(4.7 \times 10^{3} + 1 \times 10^{3})$$
   $$= 2.31V$$

Voltage Divider Bias circuit:-

1. Make wiring connections for small signal voltage divider biases circuit as per wiring diagram which is provided at the end of this experiment.

2. Ensure that the trainer is switched off & donot feed any signal at test point P15.
3. Connect a multimeter between test points P15& P20 to measure input resistance.Note down the resistance value which is the input impedance of the circuit.
4. Switch ON the trainer , set the setting on Function Generator as follows.
   Function mode – Sine
   Signal frequency – 1 KHz
   Amplitude – 250 mV
5. Observe the output signal at the test point P22 , Note down the amplitude level. Calculate voltage gain as follows.
   $\mathbf{A_V = \frac{V_{Out}}{V_{in}}}$
6. Compare the voltage gain with gain obtained in theoretical value.
   Observation:

SL NO.	NAME OF THE BIASING CIRCUIT	I_D(ma)	V_{DS}(volt)	THEORETICAL VALUE	PRACTICAL VALUE
1.	FIXED BIAS				
2.	SELF BIAS				
3.	VOLTAGE DIVIDER BIAS				

RESULT:

CONCLUSION:

PRECAUTION:

. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

VIVA-VOCE QUESTIONS:

1.What is the difference between a JFET and a bipolar transistor?

2. Explain the working of a JFET?

3. How will you determine the drain characteristics of JFET?

4. What is the difference between MOSFET and JFET

5. What is Trans-conductance?

6.What are the advantages of JFET?

EXPT NO.3

Design and simulate BJT common Emitter circuit and compare DC & AC performance.

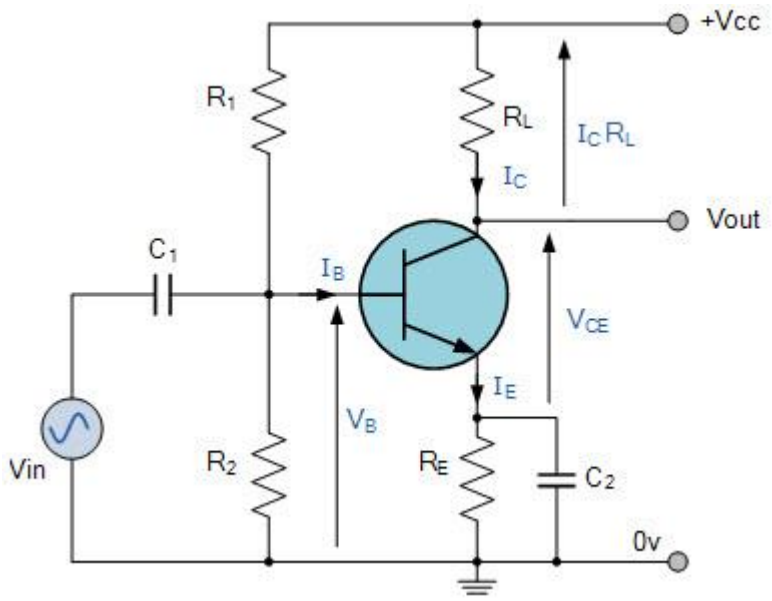
Aim Of The Experiment:

To study the AC and DC analysis of the Common Emitter Amplifier.

Equipments Needed:

Sl. No	Name of Apparatus	Specification	Quantity
1	Common emitter amplifier		
2	Patch chords		
3	CRO		

CIRCUIT DIAGRAM:



THEORY:

There are different types of electronic components in the common emitter amplifier which are R1 resistor is used for the forward bias, the R2 resistor is used for the development of bias, the RL resistor is used at the output it is called as the load resistance. The RE resistor is used for the thermal stability. The C1 capacitor is used to separate the AC signals from the DC biasing voltage and the capacitor is known as the coupling capacitor.

The figure shows that the bias vs gain common emitter amplifier transistor characteristics, if the R2 resistor increases then there is an increase in the forward bias and R1 & bias are inversely proportional to each other. The alternating current is applied to the base of the transistor of the common emitter amplifier circuit then there is a flow of small base current. Hence there is a large amount of current flow through the collector with the help of the RC resistance. The voltage near the resistance RC will change because the value is very high and the values are from the 4 to 10kohm. Hence there is a huge amount of current present in the

collector circuit which amplified from the weak signal, therefore common emitter transistor work as an amplifier circuit.

Connection Procedure:

With Bypass Capacitor:

- Connect the output of **Function Generator** to P9 & P23 terminals.
- Connect **CRO** probe at P8 & P24 terminals to measure output waveform.
- Connect the 10µf capacitor at Emitter terminal(across the Resistor).
- Connect +12V supply to P1.
- Connect P10 & P11,P14& P17,P2&P4 ,P12 & P13,P3 & P5,P6 & P7,P15 & P18,P15 & P19,P21& P22 ,P16 & P20.

Without Bypass Capacitor:

- Connect the outputof **Function Generator** to P9 & P23 terminals.
- Connect **CRO** probe at P8 & P24 terminals to measure output waveform.
- Connect P10 & P11,P14& P17,P2&P4 ,P12 & P13,P3 & P5,P6 & P7,P15 & P18,P16 & P20.

Experimental Procedure:

- Connections are made as per the connection procedure(For with emitter bypass capacitor or without bypass capacitor.)
- Switch ON the power supply and Function Generator.
- Patch the Vcc at +12Vby using regulator power supply.
- Set the input voltage of 0.1V using Function Generator and observe the output waveform.
- Calculate the gain , input impedance, output impedance and dc operating point with the given respective formulas and compare with the standard results(for with and without Bypass Capacitor

Result:

Hence studied the DC and AC analysis of Common Emitter Amplifier

Note:

The operating frequency is 1KHZ – 10KHz.

Practically:

SL NO.	Input voltage	Output voltage	A_v
1.With bypass capacitor			
2.Without bypass capacitor			

Note 1: The difference between without and with Bypass capacitor is :-

- The gain will be decreased in without By Pass Capacitor.
- Input impedance will be increased. There won`t be any effect on output impedance and DC operator point.

Note 2:

- Use Function generator in 600**Ω** mode.(Where 600 **Ω**isthe internal resistance of function generator.)

TABULATION

Standard Results

SL NO.	Z_i	Z_0	**Av**	Phase shift
1.Common Emitter				
2.Common Collector				
3.Common Base				

RESULT:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

VIVA-VOCE QUESTION:

1.Why common emitter amplifier is commonly used in amplifier circuit?

2.What are the characteristics of common emitter amplifier?

3.What is the gain of common emitter amplifier?

4.How does a common emitter amplifier work?

5.Why the common emitter amplifier gain decreases without bypass capacitor?

Experiment NO. 4

Design and simulate JFET/MOSFET common Drain circuit and compare DC & AC performance.(Study of DC & AC analysis of common drain amplifier.)

Aim Of The Experiment:-

To design a common drain (JFET) amplifier circuit & determination of voltage gain, input impedance, Output impedance of the circuit.

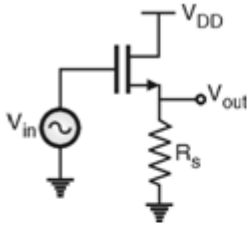
APPARATUS REQUIRED:-

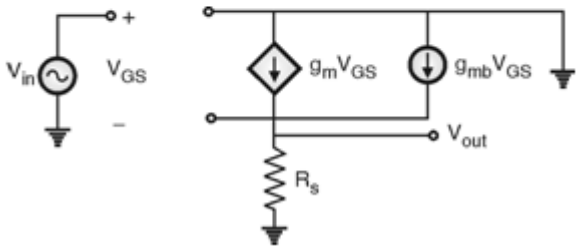
Sl. No	Name of Apparatus	Specification	Quantity
1	Common drain JFET Amplifier kit		
2	Patch chords & probe		
3	Multimeter		

Formula to be Used:-

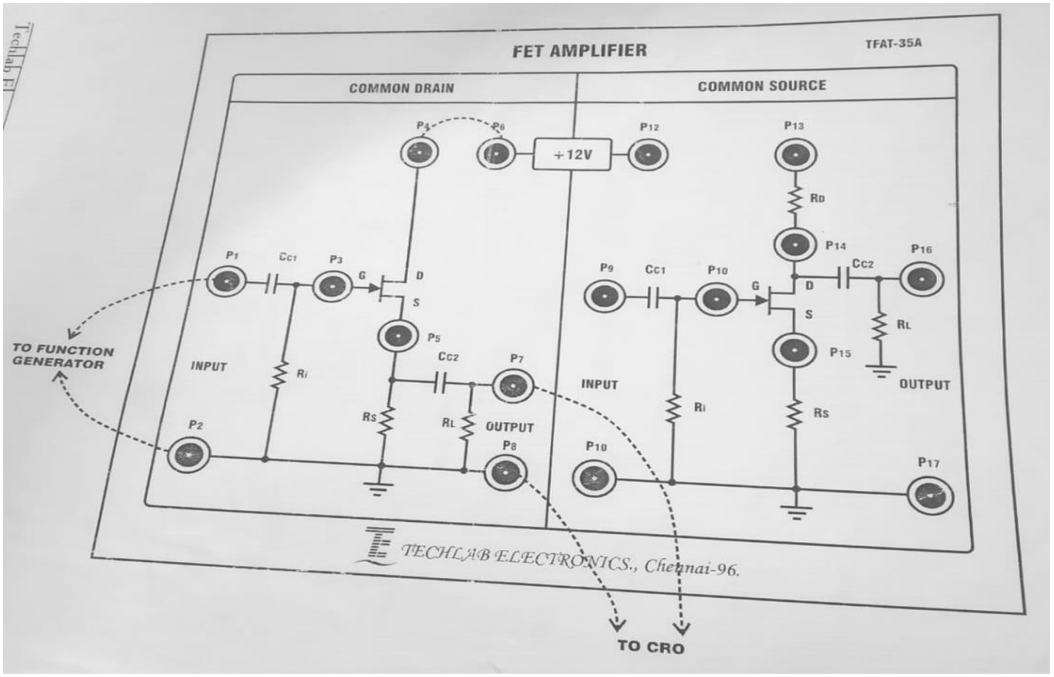
1. Trans-conductance , $g_m = g_{m0}(1-\frac{V_{GS}}{V_P})$
2. $r_d = \frac{1}{Y_{os}}$
3. Input impedance , $Z_i = R_G$
4. Output impedance , $Z_0 = r_d \| R_S \| 1/g_m$
5. Voltage gain, $A_V = \frac{g_m R_S}{1+g_m R_S}$

CIRCUIT DIAGRAM:





CONNECTION DIAGRAM:



PROCEDURE:

a. DC analysis of common Drain Amplifier.

a. Connect a multimeter (in DC current mode) or DC ammeter between test points P4 and P6 to measure the drain current.

b. Connect another one multimeter between testpoint P3 and P5 to measure gate to source voltage drop for the JFET.

c. Switch ON the trainer and donot feed any signal or voltage to the input test point(P1) of the common drain circuit.

d. The FET is biased using drain voltage, source resistance (R_S) and input resistance (R_i).Note down the Drain current from first multimeter or ammeter ,and gate to source voltage from the second multimeter.

e. Connect the multimeter between test point P5 and GND (P8), Measure the source voltage.

f. Connect the multimeter between drain and source terminal of the FET, test

point P4 and P5. Measure the drain to sources voltage.

g. Switch off the trainer ,Measure the resistance between Gate and GND terminal of the FET. Note down resistance value called input impedance of the circuit.

MODEL CALCULATION:

Given ,V_P = -8V, I_{DSS} = 9mA , Y_{OS} = 10µmhos,R_S = 4.7KΩ

a. $g_m = g_{m0}(1-\frac{V_{GS}}{V_P})$

$g_{m0} = \frac{2I_{DSS}}{V_p} = 2.2\text{ms}$

$g_m = 2.2\times10^{-3}(1-(\frac{-V_{GS}}{-8}))$ **V_{GS} is measured from Experiment**

g_m = ----------

b. $r_d = \frac{1}{Y_{os}} = \frac{1}{10\times10-6}K \cong 100K\Omega$

c. Input impedance , $Z_i = R_i$ = 1MΩ

d. Output impedance , $Z_0 = r_d \| R_S \| 1/g_m$

$Z_0 = 100 \times 10^3 \| 4.7\times 10^3 \| 1/g_m$

Z_0 =_____Ω

Voltage gain, $A_V = \frac{g_m R_S}{1+g_m R_S}$

g_m = Transconductance, R_S = 4.7 KΩ

A_V =_____

B.ACanalysis of common Drain Circuit.

a. Make wiring connections as per in wiring diagram.

b. Do following settings on Function Generator.

Function – Sine

Signal frequency – 1KHZ

Voltage – 0.25V_{PP}

c. Note down the Function Generator settings , measure the output Sine wave amplitude from oscilloscope and notedown.

d. Calculate voltage gain as follows ,$A_V = \frac{V_{out}}{V_{In}}$

e. Compare the AC signal gain with the gain obtained in DC analysis , both are nearly equal.

C. Frequency Responsesof the Amplifier:-

a. Make wiring connections as per in wiring diagram.
b. Do following settings on Function Generator.
   Function – Sine
   Signal frequency – 1KHZ

   Voltage – $1V_{PP}$
c. Note down the output sine wave voltage from oscilloscope, increase the function generator frequency in terms of 1KHZ upto10KHZ . Note down the corresponding output voltage.
d. Increase the function generator frequency in steps of 10KHZ. Notedown the output sine wave amplitude and further increase sinewave frequency in steps of 100KHZ upto 1MHZ, Notedown the output sine wave amplitude.
e. Tabulate the readings and plot the graph on semilog sheet from frequency V_S Gain.

TABULATION:

Input Voltage=_____V_{PP}

Freequency(KHZ)	**Output Voltage(V)**	**Gain = -20log($\frac{V_{out}}{V_{In}}$)dB**

RESULT:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

Viva Questions

1.What is the difference between JFET and MOSFET?

2.What is the difference between D-MOSFET and E-MOSFET?

3.Write down SCHOCKLEY'S equation?

4.Write down the characteristics equation for E-MOSFET?

EXPERIMENT NO. 05

Objective:

To study the frequency response of Common Emitter Amplifier and calculate its Bandwidth.

Components:

S.No.	Name	Quantity
1	Transistor BC107	1(One) No.
2	Resistors (100K%u2126, 10K%u2126, 1K%u2126)	1(One) No. Each
3	Resistors (2.2 K%u2126)	2(Two) No.
4	Capacitors (10µF)	2(Two) No.
5	Capacitors (100µF)	1(One) No.
6	Bread board	1(One) No.

Equipment:

S.No.	Name	Quantity
1	Dual DC Regulated Power supply (0 – 30 V)	1(One) No.
2	Cathode Ray Oscilloscope (CRO) (0-20MHz)	1(One) No.
3	Function Generator (0-1MHz)	1(One) No.
4	Connecting wires (Single Strand)	

Theory:

The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification.

Resistors R1 and R2 form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and ensure that emitter-base junction is operating in the proper region.

In order to operate transistor as an amplifier, biasing is done in such a way that the operating point is in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design V_{CE} is always set to $V_{CC}/2$. This will confirm that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. For the maximum input signal, output is produced without any distortion and clipping.

The Bypass Capacitor:

The emitter resistor R_E is required to obtain the DC quiescent point stability. However the inclusion of R_E in the circuit causes a decrease in amplification at higher frequencies. In order to avoid such a condition, it is bypassed by a capacitor so that it acts as a short circuit for AC and contributes stability for DC quiescent condition. Hence capacitor is connected in parallel with emitter resistance.

$$X_{CE} << R_E$$

$$\frac{1}{2\pi f C_E} << R_E, \quad C_E >> \frac{1}{2\pi f R_E}$$

The Input/ Output Coupling (or Blocking) Capacitor: An amplifier amplifies the given AC signal. In order to have noiseless transmission of a signal (without DC), it is necessary to block DC i.e. the direct current should not enter the amplifier or load. This is usually accomplished by inserting a coupling capacitor between two stages.

$XC_C << (R_i h_{ie})$

$$\frac{1}{2\pi f C_C} << R_i h_{ie}$$

$$C_C >> \frac{1}{2\pi f (R_i h_{ie})}$$

C_C - Output Coupling Capacitor

C_B - Input Coupling Capacitor

Frequency response of Common Emitter Amplifier:

Emitter bypass capacitors are used to short circuit the emitter resistor and thus increases the gain at high frequency. The coupling and bypass capacitors cause the fall of the signal in the low frequency response of the amplifier because their impedance becomes large at low frequencies. The stray capacitances are effectively open circuits.

In the mid frequency range large capacitors are effectively short circuits and the stray capacitors are open circuits, so that no capacitance appears in the mid frequency range. Hence the mid band frequency gain is maximum.

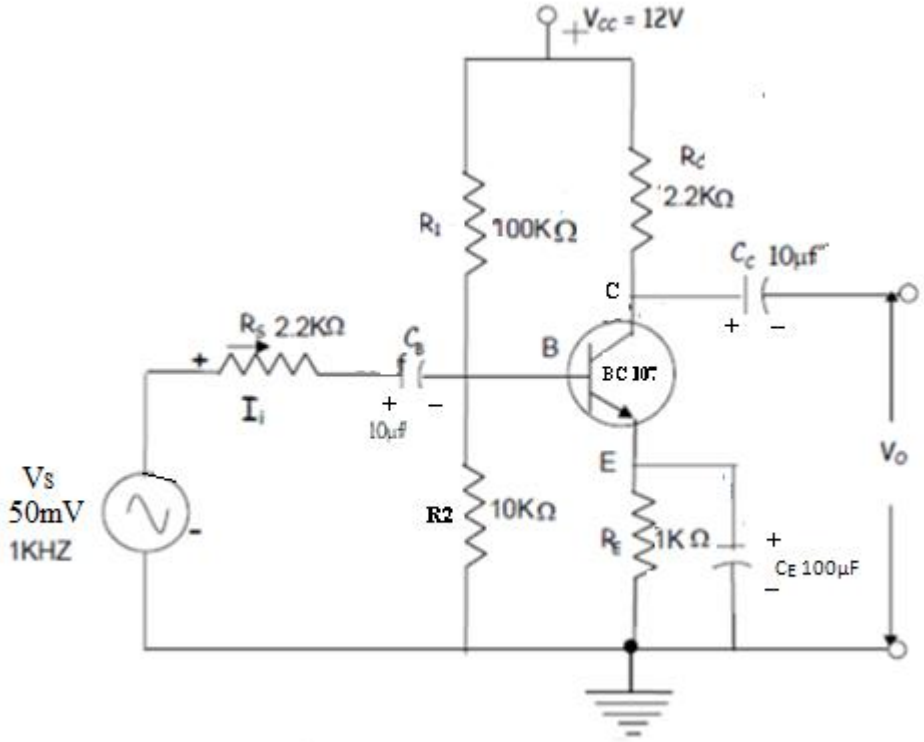
At the high frequencies, the bypass and coupling capacitors are replaced by short circuits. The stray capacitors and the transistor determine the response.

Characteristics of CE Amplifier:

1. Large current gain.
2. Large voltage gain.
3. Large power gain.
4. Current and voltage phase shift of 180^0.

5. Moderated output resistance.

Circuit Diagram:

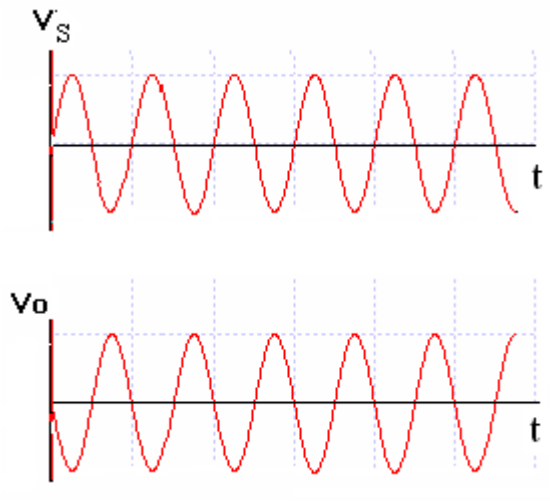


Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Set source voltage V_S = 50mV (say) at 1 KHz frequency using the function generator. Observe the phase difference between input and output by giving these two signals to the dual channels of CRO.
3. Keeping input voltage constant, vary the frequency from 50 Hz to 1 MHz in regular steps and note down the corresponding output voltage. Calculate gain in dB as shown in the tabular column.
4. Plot the graph: gain (dB) verses Frequency on a semi log graph sheet.
5. Calculate the 3-dB bandwidth from the frequency response.

Expected waveform:

(a) The Input & Output Waveforms at 1 KHz



(b) Frequency Response Curve

In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain (|A| max). These are shown as f_L and f_H and are called as the 3dB frequencies (Lower and Upper Cut-Off Frequencies respectively). The difference between higher cut-off and lower cut-off frequency is referred to as bandwidth (f_H - f_L).

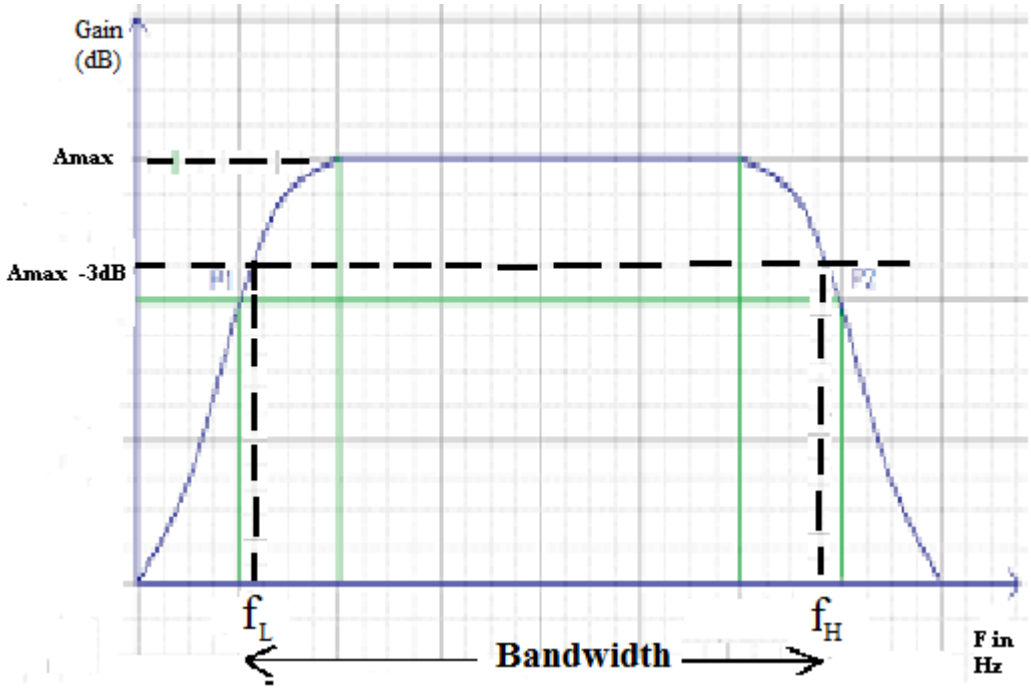


Fig: Frequency Response Curve

Calculations from the graph

Bandwidth = f_H – f_L (in Hz)

Observation tables:

V_S = 50mV

Frequency	Vo(Volts)	Gain = Vo/Vs	Gain(dB) = 20 log(Vo/Vs)

Result:

Common Emitter Amplifier is studied and its Bandwidth is calculated.

1. Maximum Gain (A_{max}) = _____ dB
2. 3dB Gain = _____ dB
3. 3dB Lower cut-off frequency, f_L = _____ Hz
4. 3dB Upper cut-off frequency, f_H = _____ Hz
5. 3dB Bandwidth (f_H - f_L) = _____ Hz

Outcomes: Students are able to

1. Calculate the Bandwidth of BJT Common Emitter amplifier.

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

Discussion/Viva Questions:

1.What is the equation for voltage gain?

2.What is cut off frequency? What is lower 3dB and upper 3dB cut off frequency?

3. What are the applications of CE amplifier?

4. What is active region?

5. What is Bandwidth of an amplifier?

6. What is the importance of gain bandwidth product?

7. Draw h parameter equivalent circuit of CE amplifier.

8. What is the importance of coupling capacitors in CE amplifier?

9. What is the importance of emitter by pass capacitor?

10. What type of feedback is used in CE amplifier?

11. What are the various types of biasing a Transistor?

12. What is Q point of operation of the transistor? What is the region of operation of the transistor when it is working as an amplifier?

13. Why frequency response of the amplifier is drawn on semi-log scale graph?

14. If Q point is not properly selected, then what will be the effect on the output waveform?

15. What are the typical values of the input impedance and output impendence of CE amplifier?

EXPERIMENT NO.6:-

To study the operation of Differential Amplifier

Apparatus Required:

Sl. No	Name of Apparatus	Specification	Quantity
1	**Differential amplifier trainer kit**		
2	**oscilloscope**		
3	**Patch chords**		

Procedure:

1. Connect +12V & -12V power supplies at their indicated position from DC Voltage Supply to
Differential Amplifier and as well as connect ground.

2. Now switch On the supply.

3. Using the '**Frequency Control'** and '**Amplitude Control'** knobs of the Function Generator, set the
input signal at 1VppVoltage, 10 KHz frequency and observe it on Oscilloscope.

4. Now connect the **Output** of Function Generator with **Vin1** of Differential Amplifier & their **Gnd**also.

5. Also connect **Vin2** to **Gnd**as shown in figure

Now connect the oscilloscope between**Vout1** and **Gnd**in order to observe the waveform & note the
amplitude of waveform which is **Vo**.

7. Now connect the oscilloscope between**Vout2** and **Gnd**& observe that you will get waveform same as
Vout1.

8. Observe the gain on both sides. It will be near about same using following formula:
Gain, Ad = Vo/Vin……..……**Eqn. 1**

9. Now remove the all patch cords & repeat the step1 to step3.

10. Now connect the **Output** of Function Generator with **Vin2** of Differential Amplifier & their **Gnd**also.

11. Also connect **Vin1** to **Gnd**as shown in figure 11.

12. Now connect the oscilloscope between**Vout2** and **Gnd**in order to observe the waveform & note the
amplitude of waveform which is **Vo**.

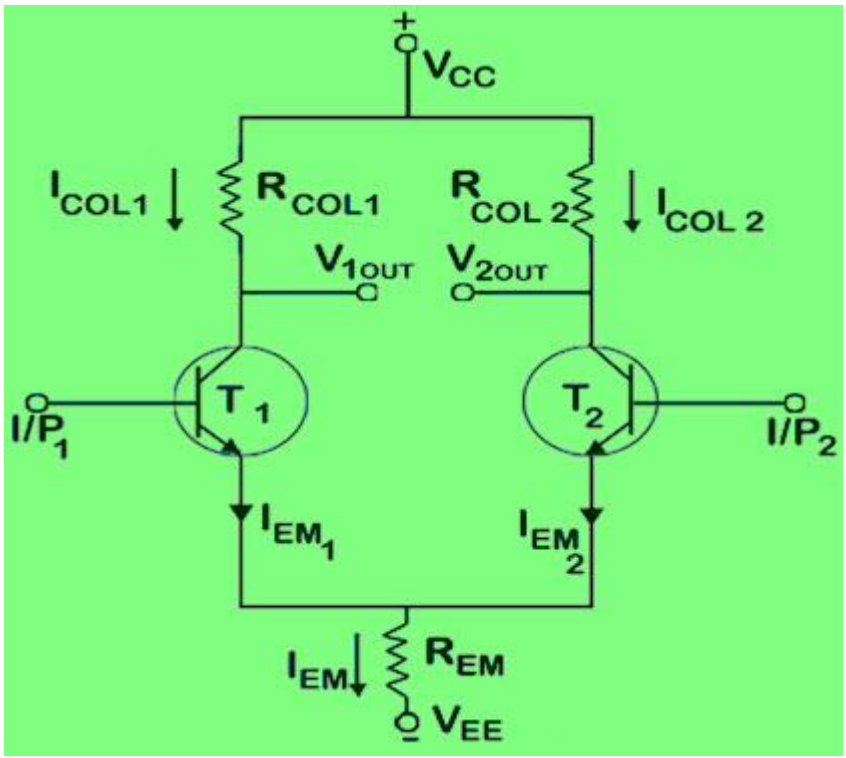
13. Now connect the oscilloscope between**Vout1** and **Gnd**& observe that you will get waveform same as
Vout2.

14. Observe the gain on both sides. It will be near about same using above equation 1.

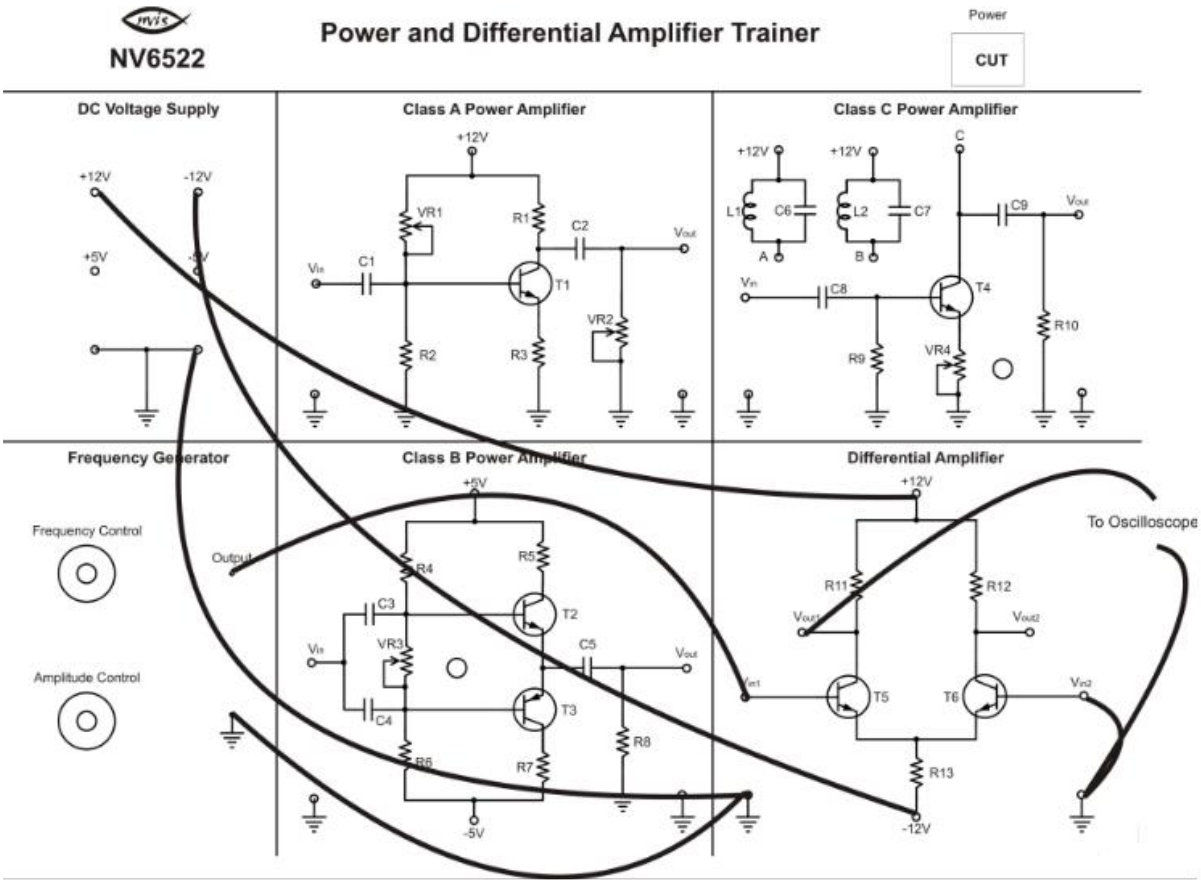
15. Now remove the all patch cords & repeat the step1 to step3.
16. Now connect the **Output** of Function Generator with both **Vin1** &**Vin2** of Differential Amplifier &
their**Gnd**also, as shown in figure12

17. Observe the output at **Vout1** &**Gnd**. Also, at **Vout2** and **Gnd**using oscilloscope. You will find there
is no signal at output. The reason is that the difference of the two signals will be equal to zero.
Practically there will be some small voltage shown across them, it is due the common mode gain (Ac)
in differential amplifier.

CIRCUIT DIAGRAM:



Connection diagram



OBSERVATION TABLE:

SL NO.	VIN	VOUT	GAIN=(VOUT/VIN) IN DB

RESULT:

CONCLUSION:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

Viva questions:

1.What are the features of differential amplifier?

2.What are differential gain and common mode gain of a differential amplifier

Experiment No. 7

Study of Darlington connections and current mirror circuits.

Aim Of The Experiment:-

7 (a) Study the characteristics of Darlington pair Class B Amplifiers.

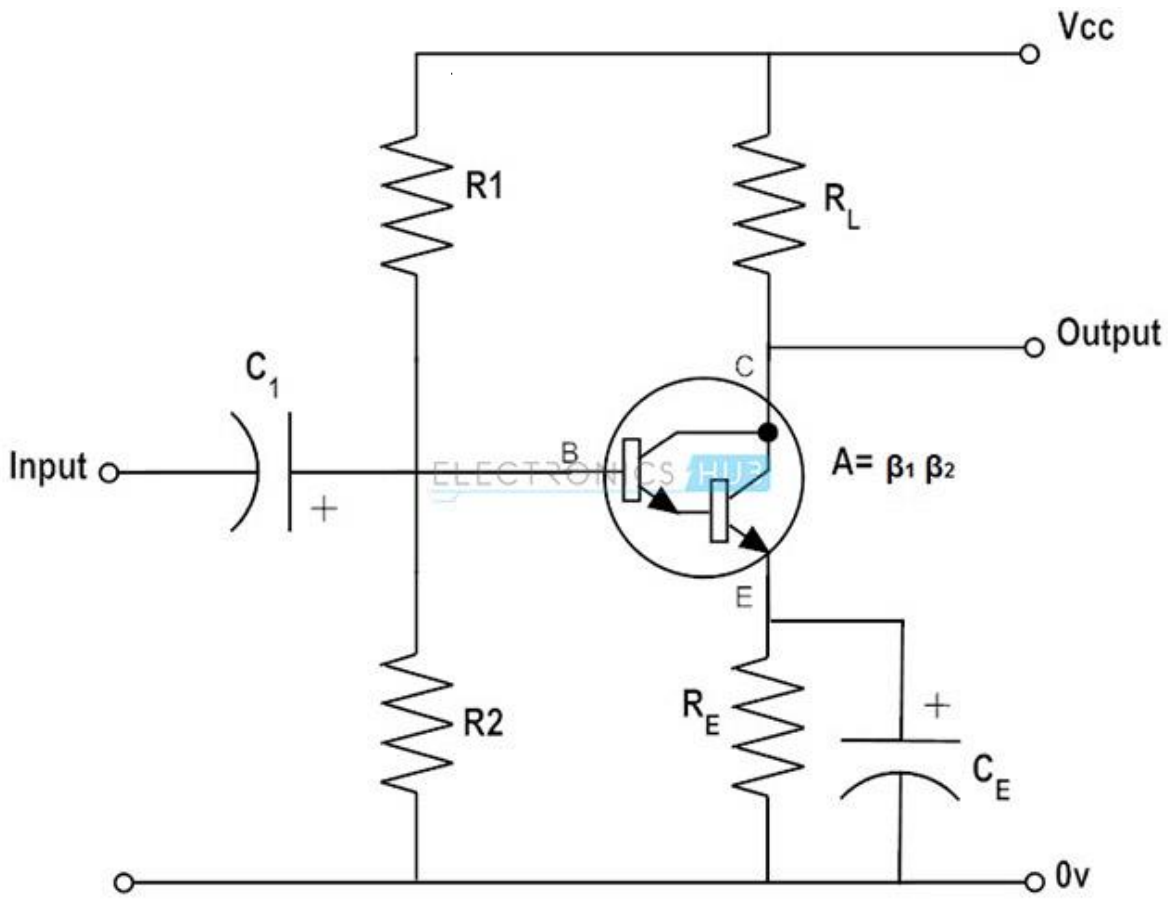
Equipments Needed:

Sl. No	Name of Apparatus	Specification	Quantity
1	Darlington Amplifier Trainer kit	TCSA-01	
2	Multimeter		
3	Patch chords	2mm	

Formula Used:

$$\%n = \frac{\pi}{4} \cdot \frac{V_L(P)}{V_{CC}} \times 100\%$$

Circuit diagram:

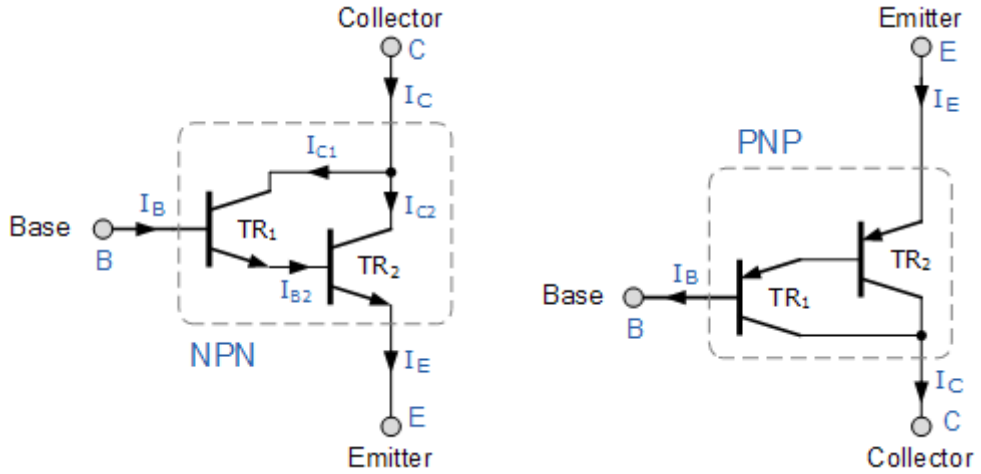


THEORY:

A **Darlington Transistor** configuration, also known as a "Darlington pair" or "super-alpha circuit", consist of two NPN or PNP transistors connected together so that the emitter current of the first transistor TR_1 becomes the base current of the second transistor TR_2. Then transistor TR1 is connected as an emitter follower and TR2 as a common emitter amplifier as shown below.

Also note that in this Darlington pair configuration, the collector current of the slave or control transistor, TR1 is "in-phase" with that of the master switching transistor TR2.

Basic Darlington Transistor Configuration



Using the NPN Darlington pair as the example, the collectors of two transistors are connected together, and the emitter of TR_1 drives the base of TR_2. This configuration achieves β multiplication because for a Base current i_b, the collector current is $\beta * i_b$ where the current gain is greater than one, or unity and this is defined as:

Connection Procedure:

1. Make the connections as per the circuit diagram.
2. Apply the Sine wave input & adjust the offset to get equal positive & negative peaks.
3. Note down the output waveform .
4. Plot the graph & see the crossover distortion effect.
5. Calculate the efficiency using the formula given.
6. Connect FG to P2- P28(1v), CRO to P35-P36.
7. Connect(+Vcc) P27-P1 , (-Vcc) P29- P3.
8. Connect P16 – P18, P17- P20 , P6 – P12, P7 – P15 , P19 – P21, P19 – P35, P28- P36.

Results:

Thus the characterstics **Darlington connections** has been studied.

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

Viva Questions

1.Draw the Darlington emitter follower circuit?

2.What are the advantages of Darlington amplifier?

OBJECTIVE:

7.(b) To study the Current Mirror circuit.

Equipments Needed:

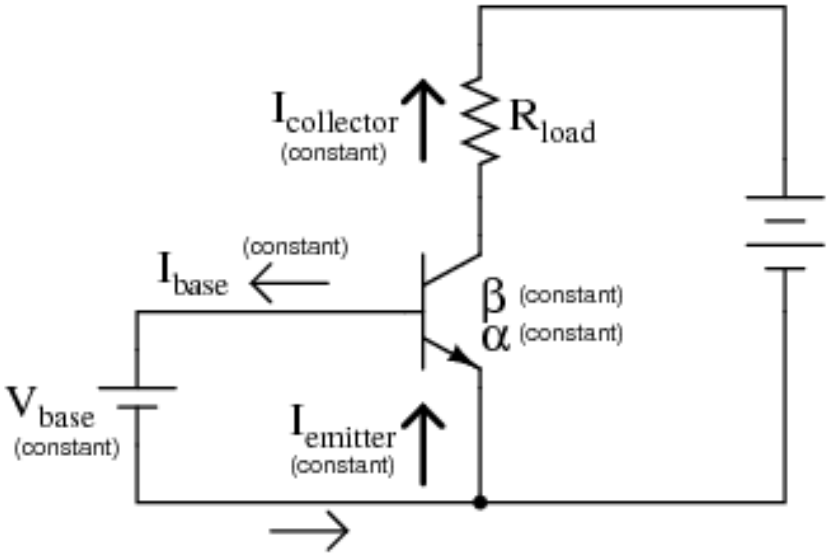
Sl. No	Name of Apparatus	Specification	Quantity
1	Current mirror trainer kit	TCSA-01B	
2	Ammeter		
3	Patch chords	2mm	

1. TCSA-01B Trainer kit
2. Ammeter
3. Patch chords.

Formula Used:

$$I = \frac{V_{CC} - V_{BE}}{R_X}$$

CIRCUIT DIAGRAM:



THEORY:

The mirror circuit generally consists of two transistors, although other devices such as FETs can be used, and some configurations do use more than two devices in the overall circuit to obtain better performance.

The current mirror circuit gains its name because it copies or mirrors the current flowing in one active device in another, keeping the output current constant regardless of loading.

The current being mirrored can be a constant current, or it can be a varying signal dependent upon the requirement and hence the circuit.

Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well or it is a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits.

Connection Procedure :

1. Connect 30V DC to Vcc (from multimeter).
2. Connect P6 & P7,P8& P9.
3. Connect the Ammeter P1&P5 ,P3& P10 (or) P2 & P5, P4 & P10.
4. Connect GND to P11.

Experimental Procedure :

1. Switch on the power supply.(GND to GND)
2. Set the Vcc at 20v by using voltage adjustment knob.(Short +30v DC &Vcc.)
3. For measuring current Q_1,place the ammeter between P1 & P5(I_1).(I_1= 2.00 mA)
4. For measuring the current Q_2 , Connect P1&P5 & place the Ammeter between that points
5. P3 & P10. (I_2= 2.00 mA)
6. For measuring I_2 ,short P1&P5 using patch cord.
7. Calculate the current I_1 &I_2 , which is approximately equal.

Tabulation:

R_1= 10 K
R_3 = 10 K

Voltage(V)	Resistor(K)	Practical value		Theoritical
		Current(I_1)mA	Current(I_2)mA	Current(I)

Result:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

Viva Questions

1.What is current mirror circuit?

2.Why current mirror circuit is needed?

3.Why current mirror circuit is used in differential amplifier

.4.list the advantage of current mirror circuit?

Experiment No. 8

8(A) Op-Amp frequency responses and compensation.

Aim Of The Experiment:-

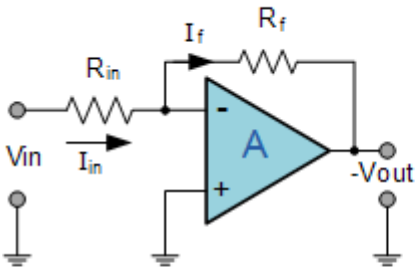
To study the frequency response of an OP-AMP without compensation.

Equipments Needed:

Sl. No	Name of Apparatus	Specification	Quantity
1	OP-AMP TRAINER KIT		
2	Function generator		
3	CRO		
4	Patch chords		

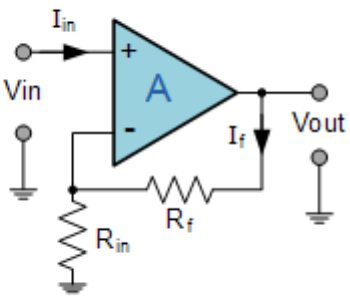
CIRCUIT DIAGRAM:

Inverting Op-amp



$$A = \frac{Vout}{Vin} = -\frac{Rf}{Rin}$$

Non-inverting Op-amp



$$A = \frac{Vout}{Vin} = 1 + \frac{Rf}{Rin}$$

THEORY:

An **Operational Amplifier** or op-amp for short, is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. These feedback components determine the resulting function or "operation" of the amplifier and by virtue of the different feedback configurations whether resistive, capacitive or both, the amplifier can perform a variety of different operations, giving rise to its name of "Operational Amplifier".

An *Operational Amplifier* is basically a three-terminal device which consists of two high impedance inputs. One of the inputs is called the **Inverting Input**, marked with a negative or "minus" sign, (–). The other input is called the **Non-inverting Input**, marked with a positive or "plus" sign (+).

A third terminal represents the operational amplifiers output port which can both sink and source either a voltage or a current. In a linear operational amplifier, the output signal is the amplification factor, known as the amplifiers gain (A) multiplied by the value of the input signal and depending on the nature of these input and output signals, there can be four different classifications of operational amplifier gain.

- Voltage – Voltage "in" and Voltage "out"
- Current – Current "in" and Current "out"
- Transconductance – Voltage "in" and Current "out"
- Transresistance – Current "in" and Voltage "out"

Since most of the circuits dealing with operational amplifiers are voltage amplifiers, we will limit the tutorials in this section to voltage amplifiers only, (Vin and Vout).

The output voltage signal from an Operational Amplifier is the difference between the signals being applied to its two individual inputs. In other words, an op-amps output signal is the difference between the two input signals as the input stage of an Operational Amplifier is in fact a differential amplifier as shown below.

PROCEDURE:

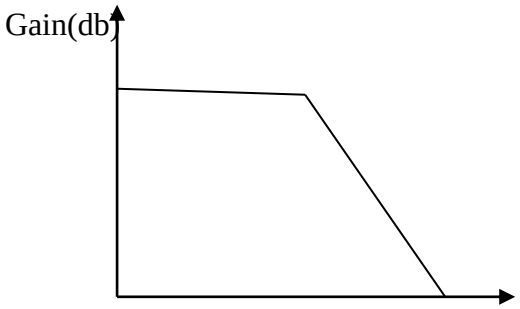
1. Connect the input sine wave from function generator to P1 & P2 terminals.
2. Connect P3 & P4, P5 & P6, P7& P8 terminals respectively.
3. Switch on the power supply.
4. Set the amplitude of Sinewave (for e.g 1v) & vary the frequency from minimum to maximum.
5. Observe the output waveform at P10 terminal.
6. Notedown the output voltage & input frequency.
7. Plot the graph between frequency VS Gain in d

TABULAR COLUMN:

Sl. No.	**Frequency(Hz)**	**Output Voltage(V)**	**Gain $A_V(V_0/V_{in})$**	**Gain in db (20 log(A_V)**
1	50			
2	100			
3	300			
4	500			
5	700			
6	1K			
7	3K			
8	5K			
9	7K			
10	10K			
11	30K			
12	50K			
13	70K			
14	100K			
15	300K			

16	500K			
17	700K			
18	1MHZ			

Model Graph:



Result:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.
3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

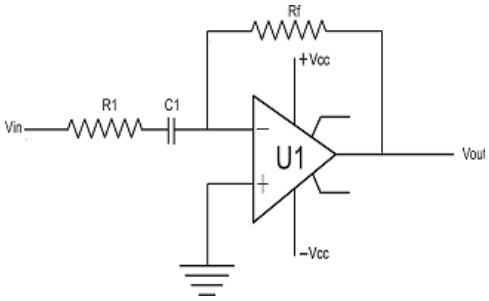
8. (B) OBJECTIVE:

To study the frequency response of an OP-AMP with compensation.

Equipments Needed:

Sl. No	Name of Apparatus	Specification	Quantity
1	Op-amp kit		
2	Function generatror		
3	CRO		
4	PATCH CHORDS		

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the input sine wave from function generator to P11 & P12 terminals.
2. Connect P13 & P14, P15 & P16 terminals respectively and for CI1 connect P17 to P21, C2 connect P18 to P21, C3 connect P19 to P21, R , connect P20 & P21.
3. Switch ON the power supply.
4. Set the amplitude of Sine wave (For e.g 1V) and vary the frequency from minimum to maximum.
5. Observe the output waveform at P22 terminal.
6. Note down the output voltage and input frequency.
7. Plot the graph between **Freequency VS Gain** in **db**. Compare the changes in graph for with compensation and without compensation.

Note:

Connect any one capacitor at a time (C1 or C2 or C3)

TABULAR COLUMN:

Sl. No.	Freequency(Hz)	Output voltage(V)	Gain A_V (V_0/V_{in})	Gain in db (20 log(A_V))

Result:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

VIVA QUESTIONS:

1. What are the ideal Characteristics of an OP-AMP ?

2. Explain the concept of virtual ground?

3. What are the internal stages in an OP-AMP IC ?

4. What type of transistor Configuration is used at the front end of an OP-AMP IC ?

5. Draw the circuit diagram of an integrator and a differentiator using an OP-AMP ?

6. Why square wave is used to test any amplifier ?

EXPERIMENT No. 09

Application of Op-Amp as differentiator , integrator ,square wave generator.

Aim Of The Experiment:

Study of Operational Amplifier as Differentiator, integrator ,square wave generator.

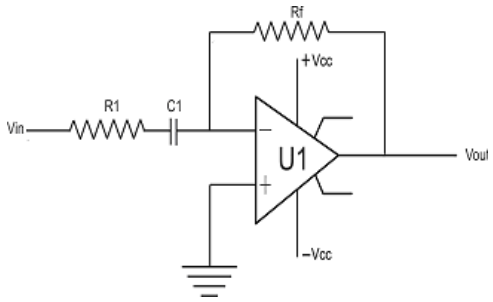
9.(A) **Objective:**

Study of Operational Amplifier as **Differentiator.**

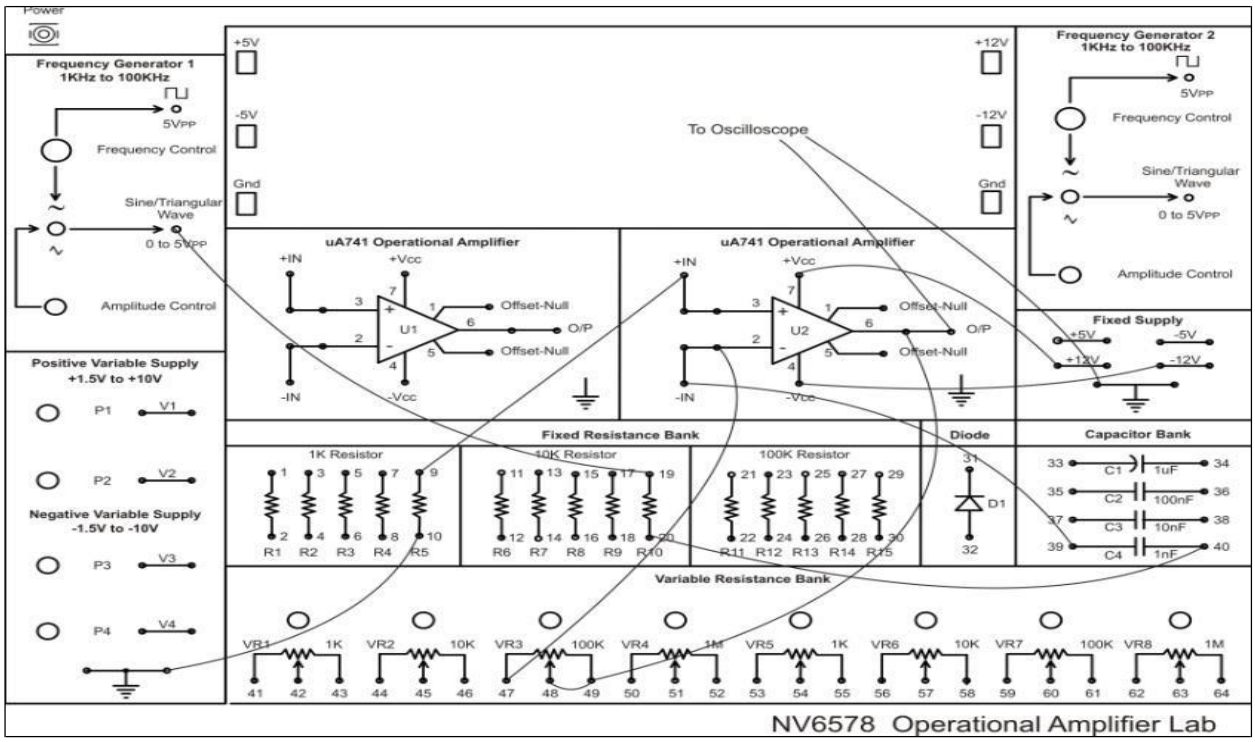
EquipmentsRequired:

Sl. No	Name of Apparatus	Specification	Quantity
1			
2			
3			

Circuit Diagram:



Connection diagram:



- Make connections according to connection diagramprovided.
- You can also perform this experiment with sine wave or square wave with 5Vpp fixed.
- You can use any FrequencyGenerator.

Theory:

Differentiator:

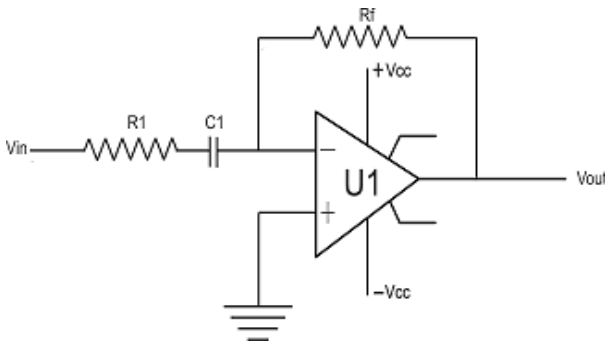
A differentiator circuit produces an output that is proportional to the derivative or rate of change of the input voltage over time. Differentiator circuit can be constructed as shown using an operational amplifier, a resistor, and a capacitor. Unlike an ideal integrator circuit where the slightest DC offset in the input eventually drives the output into saturation, for the differentiator we need not be concerned about a DC offset in the input since the derivative of a constant is always zero.

For this circuit, it can be shownthat:

Differentiator differentiates the signal over time

Vout = -RC dVin / dt

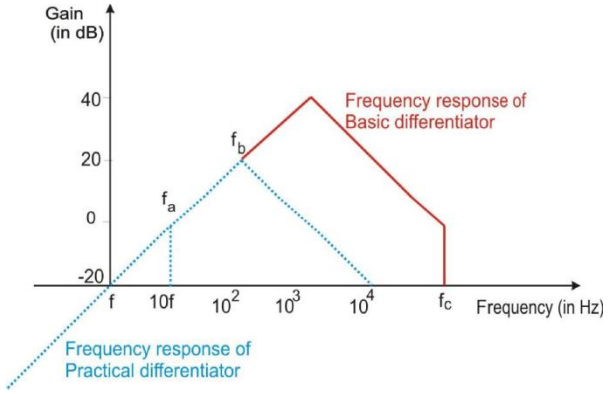
(Where Vin and Vout are functions of time.)



Differentiator circuit

Since the output voltage of a differentiator is proportional to the input frequency, high frequency signals (such as electrical noise) may saturate or cutoff the amplifier. For this reason a resistor is placed in series with the capacitor in the input as shown in Figure. This establishes high frequency limit beyond which differentiation no longer occurs.

Frequency Response of Differentiator



Frequency vs. Gain response of differentiator

Where,

$f_a = 1/ 2\pi R_f C1$

(frequency at which gain is 0 dB)

&

$f_b = 1/ 2\pi R_1 C1$ (Gain limiting frequency)

With in frequency range f to f_b gain increases at 20 dB/decade.

Procedure:

1. Connect **+12V** Fixed Power Supply to **+Vcc**and **–12V** to **–Vcc**of **U2** uA741 OperationalAmplifier.
2. Set triangular wave at 5 KHz with 5 Vpp using amplitude & frequency control knobs from **Frequency Generator1**.
3. Applytriangularwavetoterminal**19**of**R10**andterminal**20**toterminal**40**of **C4** and terminal **39** to –**IN** of **U2.**
4. Connect terminal **9** of **R5** to **+IN** of **U2** and terminal **10** toground.
5. Short terminal **48 & 49** of **VR3.** (Initially VR3 set at fully anti clockwise position)
6. Connect **47** to **–IN** of **U2** and terminal **49** to **O/P** (Pin number 6) of**U2**.
7. Connect Oscilloscope between **O/P** (Pin number 6) of **U2** &ground.
8. In output, you will get square wave with the adjustment ofVR3.
9. Now increase the frequency using **Frequency Control** knob & observe the output wave form. After 15.9 KHz, you will get triangular waveform i.e. it is working as High PassFilter.

Note: You can control the gain of output waveform with the help of VR3.

10. Similarly you can use different combinations of R &C.

Calculation:

$$f=\frac{1}{2pRC}$$

Where,

f= Cutoff Frequency, **R**= Resistance connected in inverting terminal & **C**=Capacitance connected in inverting terminal

OBSERVATION TABLE

S.NO	R_f(kΩ)	C (µF)	V_0(mV)	Gain	Theoretical Gain

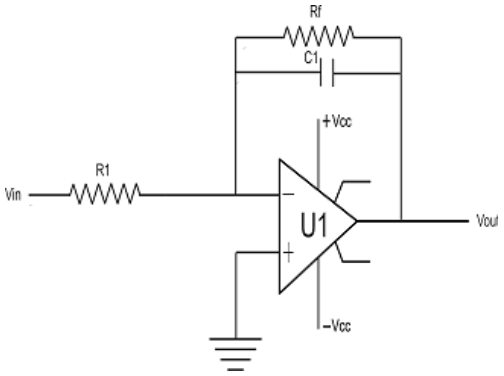
Objective:

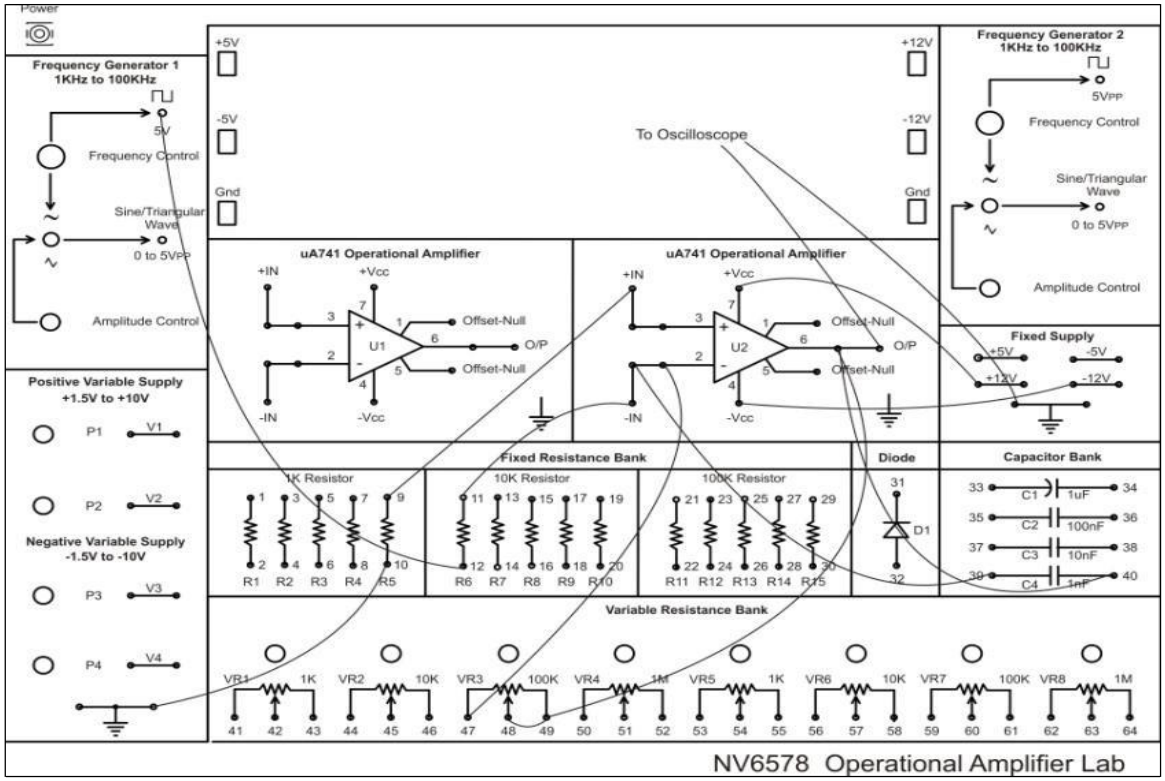
9(b)Study of Operational Amplifier as **Integrator**.

Equipments Needed:

Sl. No	Name of Apparatus	Specification	Quantity
1			
2			
3			

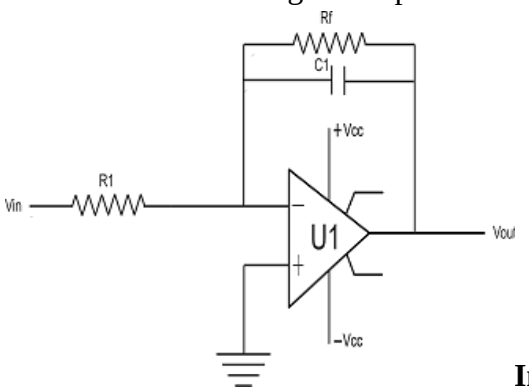
Circuit Diagram:





THEORY:

As its name implies, the **Integrator Amplifier** is an operational amplifier circuit that performs the mathematical operation of **Integration** that is we can cause the output to respond to changes in the input voltage over time. The integrator amplifier acts like a storage element that "produces a voltage output which is proportional to the integral of its input voltage with respect to time". In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through thecapacitor.



Integrator circuit

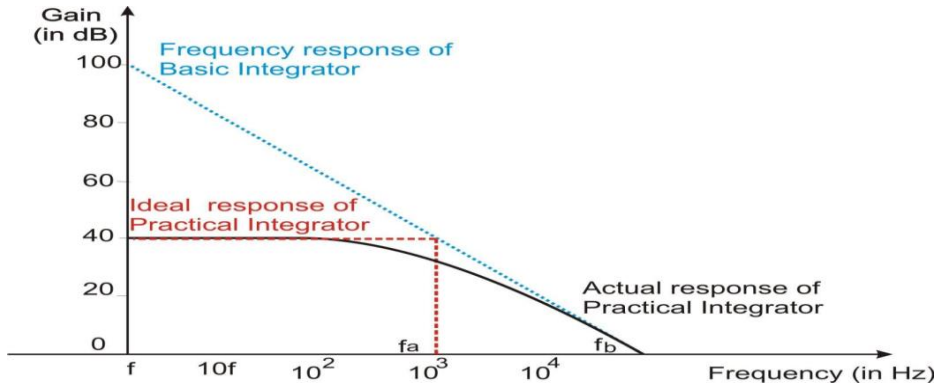
Integrates the signal over time

$$V_{out} = -\int_0^t \frac{V_{in}}{RC}\,dt - V_{initial}$$

(Where V_{in} and V_{out} are functions of time, $V_{initial}$ is the output voltage of the integrator at time $t = 0$.)

Note that this can also be viewed as a low-pass electronic filter. It is a filter with a single pole at DC (i.e., where $\omega = 0$) and gain.

Frequency Response of Integrator:



Frequency Vs gain response of Integrator

Where

$f_a = 1/ 2\pi R_f C_f$ (Gain limiting frequency)

&

fb = 1/ 2πR1 Cf (frequency at which gain is 0 dB)

With in frequency range f_a to f_b circuit works as integrator.

Procedure:

1. Connect +12V Fixed Power Supply to +Vcc and –12V to –Vcc of U2 uA741 OperationalAmplifier.
2. Set squarer wave at 2 KHz with 5 Vpp (set amplitude pot at fully clockwise direction) from Frequency Generator1.
3. Apply square wave to terminal 12 of R6 and terminal 11 to terminal -IN ofU2.
4. Connect terminal 9 of R5 to +IN of U2 and terminal 10 toground.
5. Short terminal 48 and 49 of VR3. (set VR3 at fully anti clockwiseposition)
6. Now connect 47 to –IN of U2 and terminal 49 to O/P (Pin number 6) ofU2.
7. Connect 39 terminal of C4 to -IN of U2 & terminal 40 to O/P (Pin number 6) of U2.
8. Connect Oscilloscope between O/P (Pin number 6) of U2 and ground.
9. In output, at low frequency you will get squarewave.

Note: Adjust the VR3 to obtain maximum amplified squarewave.

10. Now increase the frequency using **Frequency Control** knob &

observe the output wave form. After 15.9 KHz, you will get triangular waveform i.e. it is working as low PassFilter.

Calculation:

$$f=\frac{1}{2\pi RC}$$

Where,

f = Cutoff Frequency, R= Resistance connected in inverting terminal & C=Capacitance connected in feedback of operationalamplifier.

OBSERVATION TABLE

S.NO	R_1(kΩ)	C (μF)	V_0(mV)	Gain	Theoretical Gain

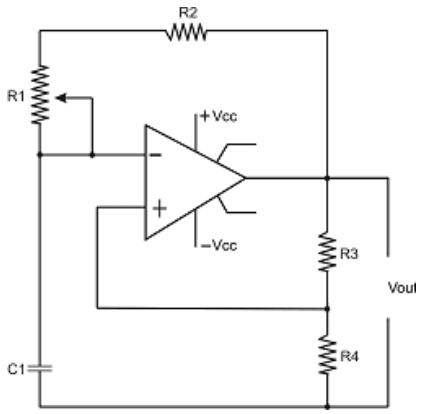
OBJECTIVE:

9(c) Study of Operational Amplifier as **Square Wave Generator.**

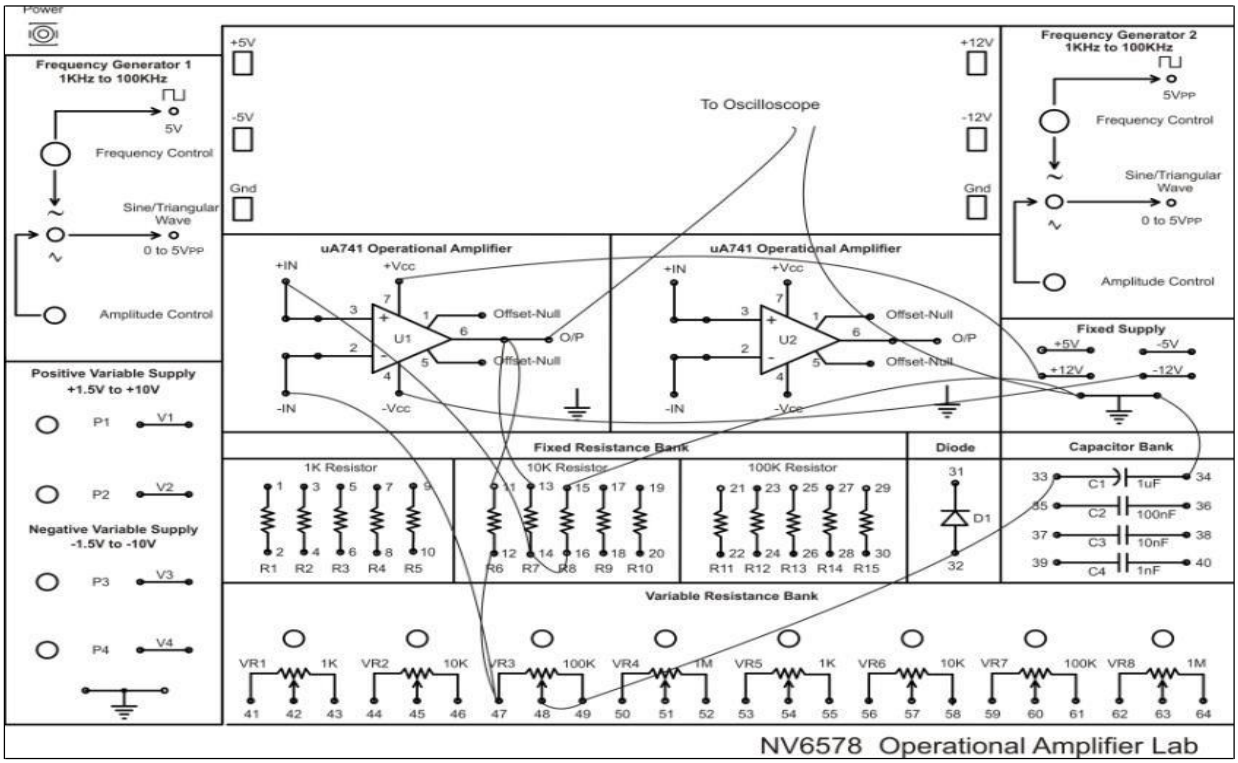
Equipments Needed:

Sl. No	Name of Apparatus	Specification	Quantity
1			
2			
3			

Circuit Diagram:



Op-Amp connection as Square Wave Generator



Note:

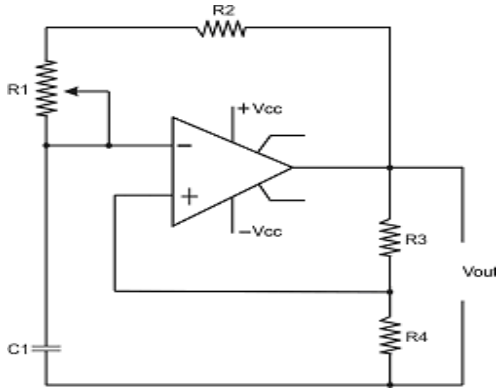
- You can select any IC, U1 orU2.
- Make connections according to connection diagramprovided.
- You can also perform above experiment with±5V.

THEORY:

Square wave is generated when op-amp is forced to operate in saturation region. i.e. the output of op-amp is forced to swing respectively between +Vsat& -Vsat resulting in generation of square wave.The square wave generator is also called free running generator or Astablemultivibrator assuming the voltage across capacitor C1 is zero at the instant the DC supply voltage at +Vcc& -Vcc are applied. Initially the capacitor acts as a short circuit. The gain of op-amp is very large hence drives the output of op- amp to its saturation.This square wave generator is like the Schmitt trigger circuit in that the reference voltage for the comparator action depends on the output voltage. This circuit is also classified as an astablemultivibrator.A wide range square wave generator using IC uA741 is shown here. The circuit uses positive feedback for Schmitt trigger action and negative feedback for timing of the waveform.

Let us presume that the output is high and the capacitor C1 is fully discharged.C1 now starts charging via R2 and R1.When the voltage across C1 rises above that the Junction of R3 & R4,the output quickly switches to fully negative voltage.C1 now starts discharging and charges in the opposite direction.Again,when the negative voltage across C1 falls below that at pin 3,the circuit switches back quickly to the fully positive output value.The cycle repeats endlessly.

The frequency of the square wave can be varied by varying POT R1.The frequency range of the circuit depends on the value of R3, R4 & C1.



(Op-amp circuit connection as Square Wave Generator)

- The frequency of output can be varied by varying POTR1.

- The frequency range can be adjusted by changing the value of R3,R4 orC1

Procedure:

1. Connect +12V fixed supply to +Vcc and -12V to –Vcc of U1uA741.
2. Connect terminal 14 of R7 to +IN of U1 and 13 to O/P (pin no. 6) ofU1.
3. Connect terminal 11 of R6 to pin no. 6 of U1 and 12 to terminal 47 ofVR3.
4. Short terminal 48 and 49 of VR3 then connect terminal 47 with –IN of U1. (Initially set VR3 at fully anti clockwisedirection)
5. Connect terminal 33 of C1 to terminal 49 of VR3 and terminal 34 toground.
6. Connect terminal 14 of R7 to 16 of R8 then terminal 15 toground.
7. Now connect Oscilloscope between O/P of U1 andground.
8. Now vary the VR3 towards clockwise direction & observe output on Oscilloscope.

Result:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

Viva Questions:

1.Define CMRR?

2.Why open-loop op-amp configurations are not used in linear applications?

3.What is a voltage transfer curve of an op-amp?

4.what are differential gain and common mode gain of a differential amplifier?

5.Define slew rate?

6.What is a voltage follower?

7.What is an inverting amplifier?

8.What is an integrator?

9.Op-amp is used mostly as an integrator than a differentiator.Why?

10.What is an summing amplifier?

Experiment No 10

RC phase shift oscillator using Op-Amp

Aim Of The Experiment:

Study of OPAMP as RC Phase Shift Oscillator and to determine frequency of oscillation.

Equipments Needed:

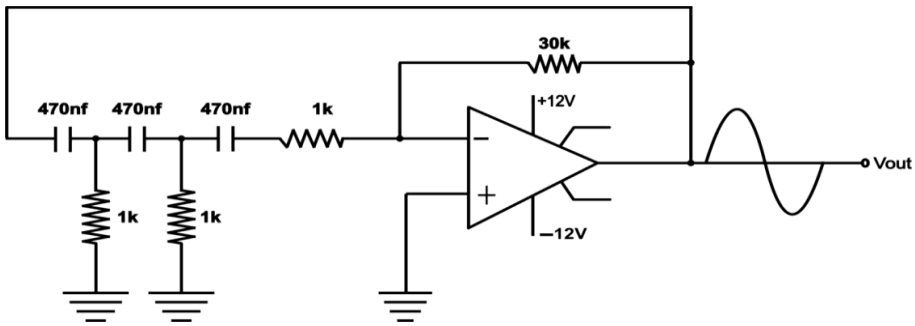
Sl. No	Name of Apparatus	Specification	Quantity
1			
2			
3			

1. PatchCords
   - 1mm to 2mm
   - 1mm to1mm
   - 2mm to2mm
2. Oscilloscope

Components Required:

1. M.F.R. ¼ **W 1K** – 3Nos.
2. M.F.R. ¼ **W 30K** – 1Nos.
3. Metallic Capacitor **470 nF**– 3Nos.
4. Metallic Capacitor **100 nF**– 3Nos.

Circuit Diagram:



Note:

- You can select any IC, U1 orU2.
- Make connections according to circuit diagramprovided.
- You can also perform above experiment with±5V.
- You can select 1 K resistances from kitalso.
- You can make 30 K resistances from series combination of on board 10 K resistances.

THEORY: ***RC phase-shift oscillators*** use resistor-capacitor (RC) network (Figure 1) to provide the phase-shift required by the feedback signal. They have excellent frequency stability and can yield a pure sine wave for a wide range of loads.

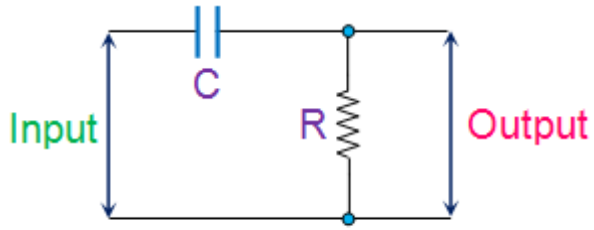


Figure 1 RC Phase-Shift Network

Ideally a simple RC network is expected to have an output which leads the input by 90°. However, in reality, the phase-difference will be less than this as the capacitor used in the circuit cannot be ideal. Mathematically the phase angle of the RC network is expressed as

$$\varphi = tan^{-1}\frac{X_C}{R}$$

Where, $X_C = 1/(2\pi fC)$ is the reactance of the capacitor C and R is the resistor. In oscillators, these kind of RC phase-shift networks, each offering a definite phase-shift can be cascaded so as to satisfy the phase-shift condition led by the Barkhausen Criterion.

One such example is the case in which **RC phase-shift oscillator** is formed by cascading three RC phase-shift networks, each offering a phase-shift of 60°, as shown by Figure 2.

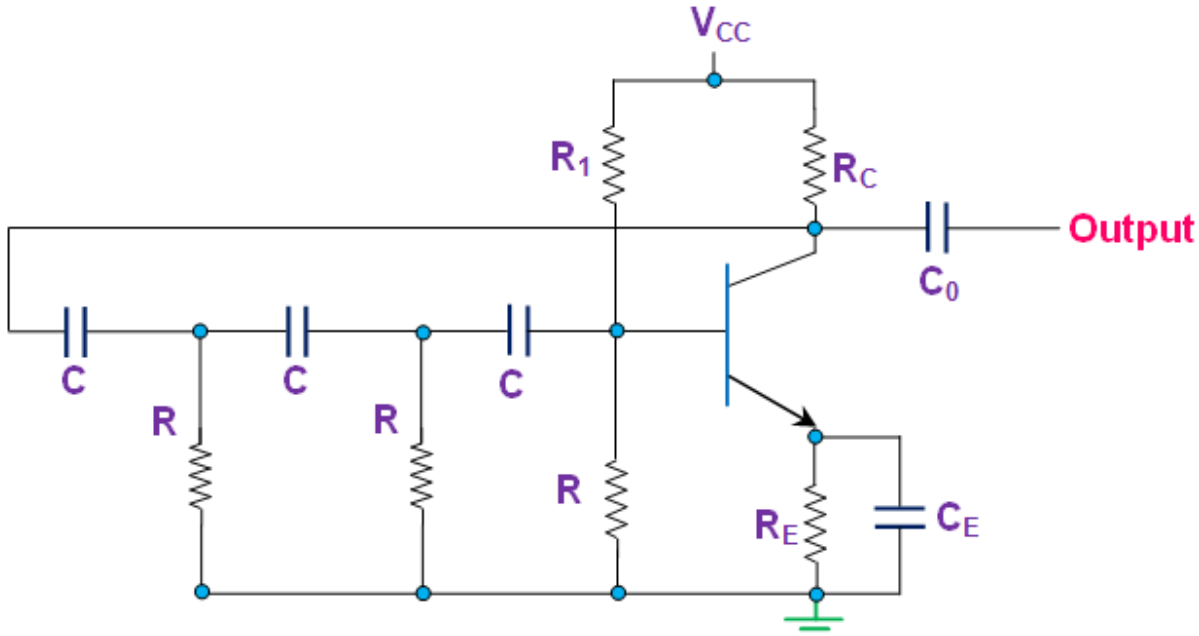


Figure 2 RC Phase-Shift Oscillator Using BJT

Here the collector resistor RC limits the collector current of the transistor, resistors R_1 and R (nearest to the transistor) form the voltage divider network while the emitter resistor $R_E$improves the stability. Next, the capacitors C_E and C_o are the emitter by-pass capacitor and the output DC decoupling capacitor, respectively. Further, the circuit also shows three RC networks employed in the feedback path.

This arrangement causes the output waveform to shift by 180° during its course of travel from output terminal to the base of the transistor. Next, this signal will be shifted again by 180° by

the transistor in the circuit due to the fact that the phase-difference between the input and the output will be 180° in the case of common emitter configuration. This makes the net phase-difference to be 360°, satisfying the phase-difference condition.
One more way of satisfying the phase-difference condition is to use four RC networks, each offering a phase-shift of 45°. Hence it can be concluded that the **RC phase-shift oscillators** can be designed in many ways as the number of RC networks in them is not fixed. However it is to be noted that, although an increase in the number of stages increases the frequency stability of the circuit, it also adversely affects the output frequency of the oscillator due to the loading effect.
The generalized expression for the frequency of oscillations produced by a **RC phase-shift oscillator** is given by

$$f = \frac{1}{2\pi RC\sqrt{2N}}$$

Where, N is the number of RC stages formed by the resistors R and the capacitors C. Further, as is the case for most type of oscillators, even the RC phase-shift oscillators can be designed using an OpAmp as its part of the amplifier section (Figure 3). Nevertheless, the mode of working remains the same while it is to be noted that, here, the required phase-shift of 360° is offered collectively by the RC phase-shift networks and the Op-Amp working in inverted configuration.

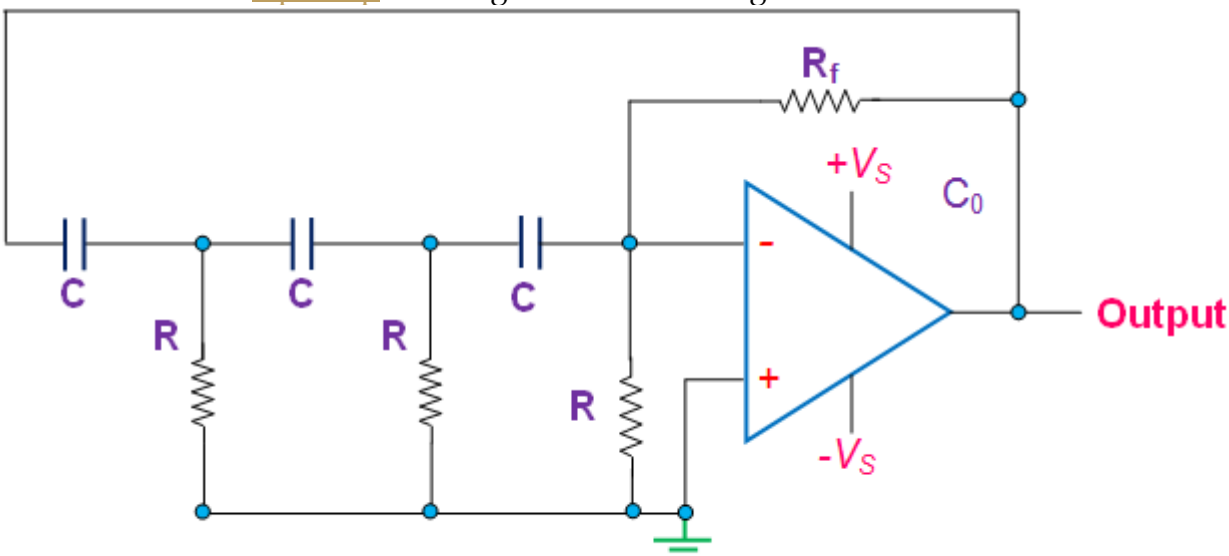
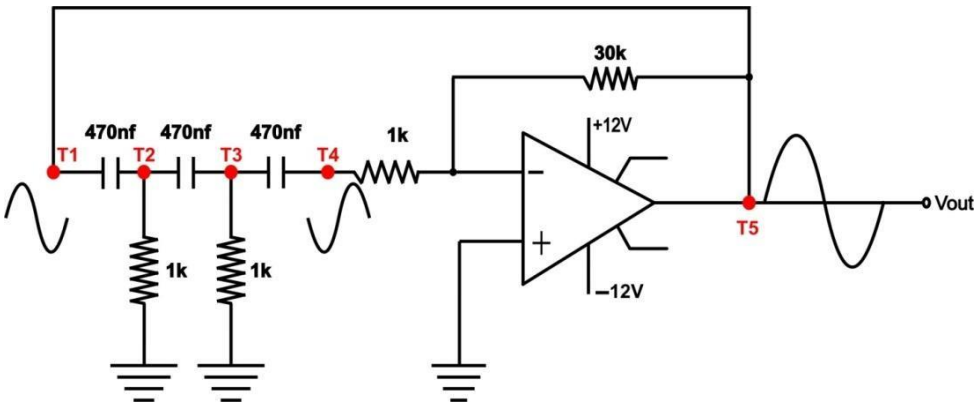


Figure 3 RC Phase-Shift Oscillator Using an Op-Amp

Procedure:

1. Connect **+12V** Fixed Power Supply to **+Vcc**and **–12V** to **–Vcc**of **U1uA741**.
2. Connect **+IN** of **U1** toground.
3. Now make connections as per above circuit diagram on breadboard.
4. Now connect Oscilloscope between **O/P** (Pin number 6) of **U1** andground.

5. Now observe output waveform as well as phase shift at points T2, T3 & T4 as shown in belowfigure.



6. Measure the frequency of output waveform and compare it with theoretical frequency.

$$\text{Frequency of oscillation :} \quad F = \frac{1}{2\pi RC\sqrt{6}}$$

Note: Spikes occur at points T3 & T4 (RC Phase Shift Network section) because of capacitive current and OPAMPsaturation.

7. Now perform this experiment with 100nF capacitor and observe the output waveform and measure frequency ofoscillation.
8. Similarly you can perform this experiment with different combination of R &C.

Observation

S. No.	Resistance(KΩ)	Capacitance(μF)	Practical Frequency(Hz)	Theoretical Frequency(Hz)
1	4.7	0.1		
2	4.7	0.01		
3	4.7	0.001		

Result:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

VIVA QUESTIONS:

1. Which type of feedback is incorporated in RC phase shift oscillator ?

2. Can we built up an RC phase shift oscillator using two stages of RC network of each 900phase shift ?

3. State Barkhausen criterion?

4. What is the condition imposed on A and □□to get sustained oscillations ?

Crystal Oscillator.

Objective:

10 (b) Study of the **Transistorized Crystal Oscillator** (1MHz).

Equipments Needed:

Sl. No	Name of Apparatus	Specification	Quantity
1			
2			
3			

Analog board,**AB114**

1. DC Power Supply 12V from externalsource.
2. Oscilloscope.
3. 2mm patchcords.

Circuit diagram:

The circuit to study the Crystal Oscillator is shown below:

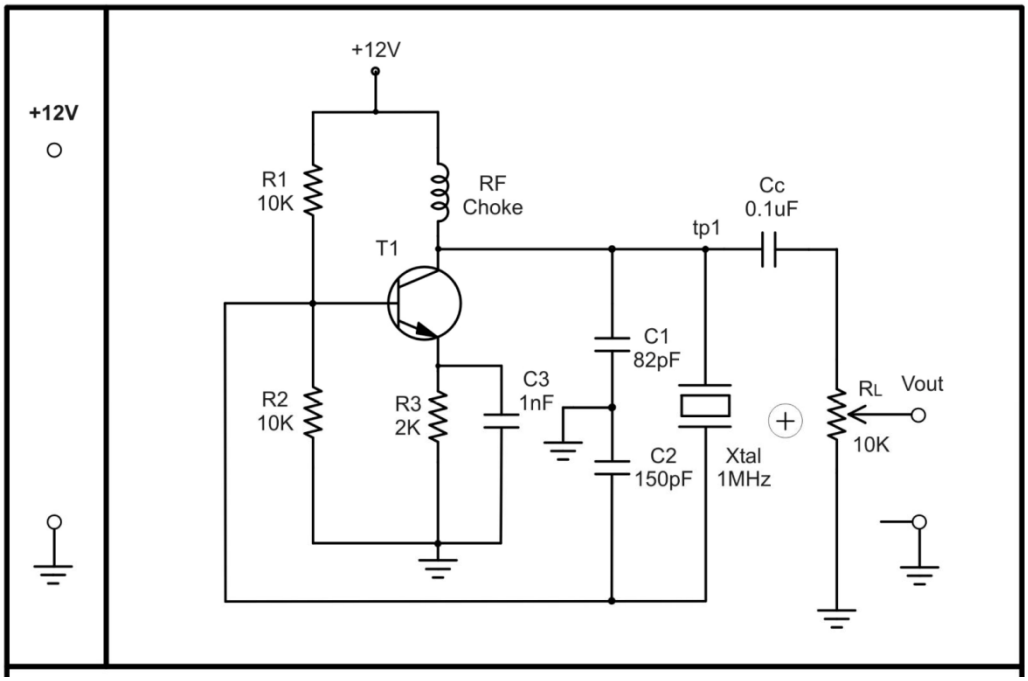


Figure 7.Circuit diagram of crystal oscillator

Crystal oscillators operate on the principle of inverse piezoelectric effect in which an alternating voltage applied across the crystal surfaces causes it to vibrate at its natural frequency. It is these vibrations which eventually get converted into oscillations. These oscillators are usually made of Quartz crystal, eventhough other substances like Rochelle salt and Tourmaline exhibit the piezoelectric effect because,

quartz is inexpensive, naturally-available and mechanically-strong when compared toothersIn crystal oscillators, the crystal is suitably cut and mounted between two metallic plates as shown by Figure 1a whose electrical equivalent is shown by Figure 1b. In reality, the crystal behaves like a series RLC circuit, formed by the components

1. A low-valued resistor R_s
2. A large-valued inductor L_s
3. A small-valued capacitor C_s

which will be in parallel with the capacitance of its electrodes C_p.

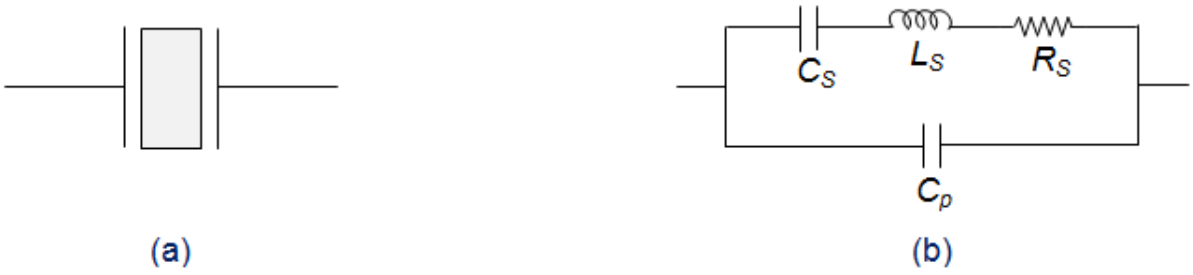


Figure 1 (a) Quartz Crystal (b) Equivalent Electric Circuit

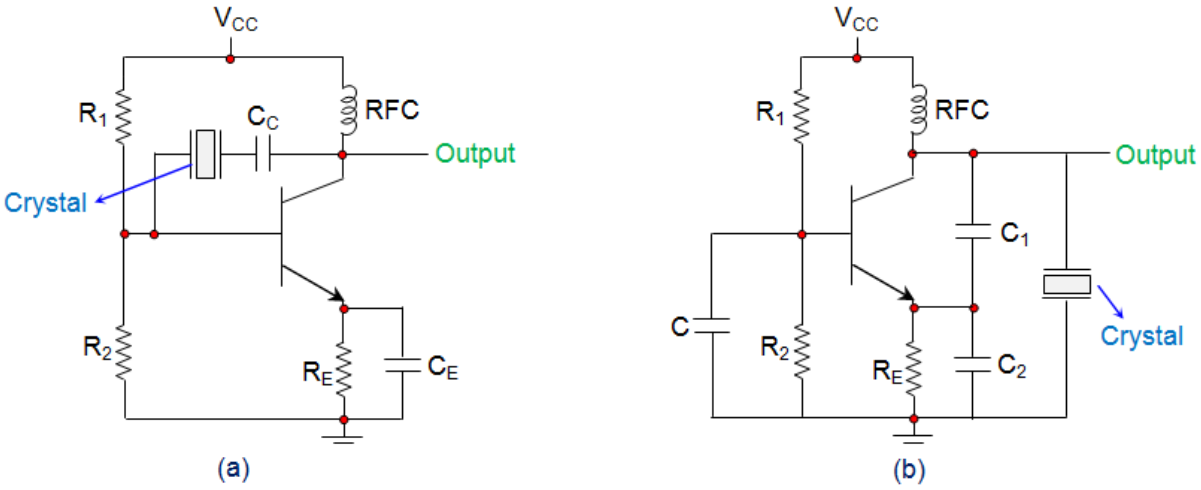


Figure 2 Crystal Oscillator Operating in (a) Series Resonance (b) Parallel Resonance

Due to the presence of C_p, the crystal will resonate at two different frequencies viz.,

1. Series Resonant Frequency, f_s which occurs when the series capacitance $C_S$resonates with the series inductance L_S. At this stage, the crystal impedance will be the least and hence the amount of feedback will be the largest. Mathematical expression for the same is given as

$$f_s = \frac{1}{2\pi\sqrt{L_s C_s}}$$

2. Parallel Resonant frequency, f_p which is exhibited when the reactance of the $L_SC_S$leg equals the reactance of the parallel capacitor C_p i.e. L_S and C_S resonate with C_p. At this instant, the crystal impedance will be the highest and thus the feedback will be the

least. Mathematically it can be given as

$$f_p = \frac{1}{2\pi\sqrt{L_S \frac{C_P C_S}{C_P + C_S}}}$$

The behaviour of the capacitor will be capacitive both below f_S and above f_p. However for the frequencies which lie in-between f_S and above f_p, the crystal's behavior will be inductive. Further when the frequency becomes equal to parallel resonant frequency f_p, then the interaction between L_S and C_p would form a parallel tuned LC tank circuit. Hence, a crystal can be viewed as a combination of series and parallel tuned resonance circuits due to which one needs to tune the circuit for any one among these two. Moreover it is to be noted that f_p will be higher than f_s and the closeness between the two will be decided by the cut and the dimensions of the crystal in-use.

Crystal oscillators can be designed by connecting the crystal into the circuit such that it offers low impedance when operated in series-resonant mode (Figure 2a) and high impedance when operated in anti-resonant or parallel resonant mode (Figure 2b).

Procedure:

- Connect +12V variable DC power supplies at the indicated position from external source or **Scientech 2612 AnalogLab.**
- Connect Oscilloscope CHI at the output socket 'V_{out}'.
- Switch 'On' the PowerSupply.
- Observe output on Oscilloscope, if there is a sinusoidal wave present than note down amplitude and frequency of the same in table givenbelow.
- If the output is not the proper sine wave rotate the pot given for Loadresistance.
- Compare the output frequency with that of quartz crystal 'XTAL' which is 1 MHz.
- Also observe the output at test point TP1 and DC output occurring at the test point.

Observation Table:

S. No.	Resonance Frequency of Tank circuit (Measured)	Frequency of Output V_{OUT}	Amplitude of Output V_{OUT}

Table 1

Calculation:

Resonance frequency of Tank circuit,**f** $= \frac{1}{2\pi\sqrt{LC}}$

Result:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

Viva Question

1. What is an oscillator?

2. What is Barkhausein criterion for oscillation?

3. What is its need?

4. Discuss the advantages of oscillator?

5. What do you understand by damped and undamped oscillation?

6. Why is crystal oscillator used in radio transmitter?

Experiment 11

Obtain the bandwidth of FET /BJT using squarewave testing of an amplifier.

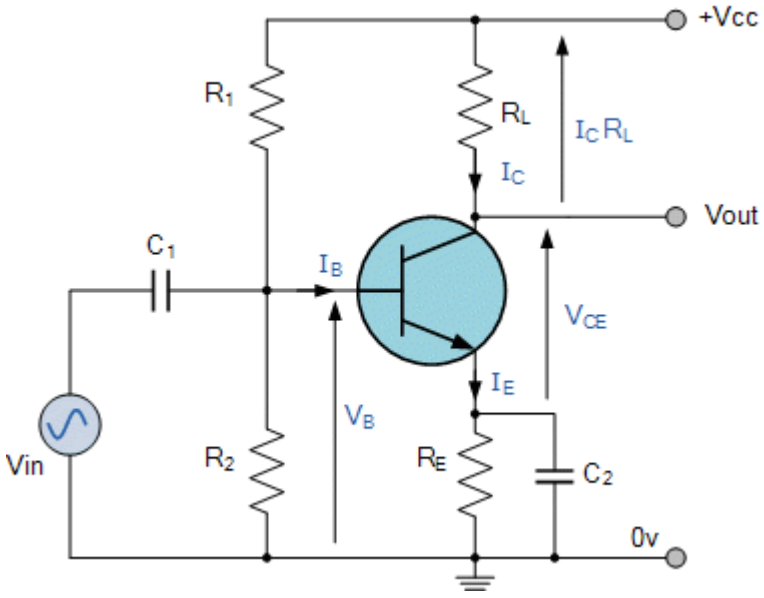
Aim Of The Experiment:-

Obtain the bandwidth of FET /BJT using square wave testing of an amplifier. To find the lower & higher cutoff frequency of an amplifier by conducting a square wave testing.

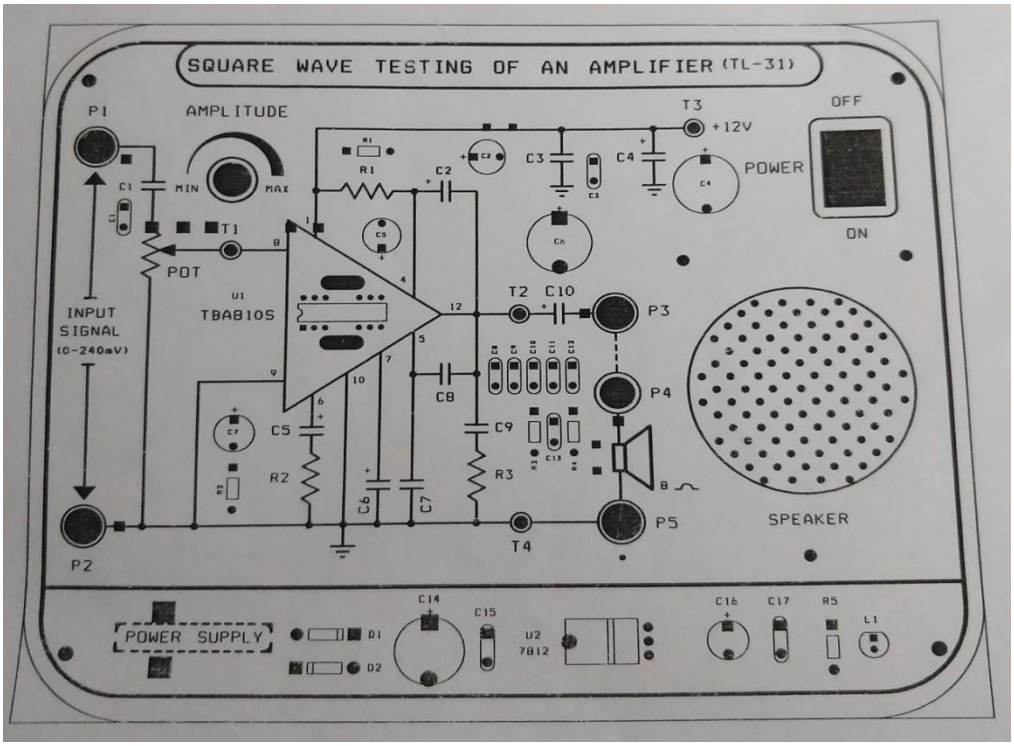
Apparatus Required:-

Sl No.	Apparatus			
1	TL – 31			
2	Function Generator			
3	CRO			

Circuit Diagram:

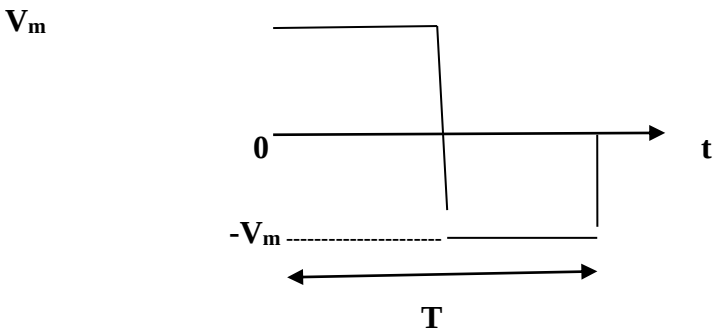


KITDIAGRAM:



Theory:

A sense for the frequency responses of an amplifier can be determined experimentally by appling a square wave signal to the amplifier & nothing the output response. The shape of the output waveform will reveal whether the high or low frequencies are being properly amplified . By use of squarewave testing is significantly less time consuming than applying a series of sinusoidal signals at different frequencies & magnitudes to test the frequency of the amplifier.The reason for choosing a squarewave signal for the testing process is best described by examining the Fourier series expansion of a square wave composed of a series sinusoidal component of different magnitudes & frequencies. The summation of the terms of the series will result in the original waveform. In other words even though a waveform any not be sinusoidal, it can be reproduced by a series of sinusoidal terms of different frequencies & magnitudes.



$$F_S = \frac{1}{T}$$

$$V = \frac{4}{\pi} V_m (\sin 2\pi f_s t + \frac{1}{3}\sin 2\pi (3f_s)t + \frac{1}{5}\sin 2\pi (5f_s)t + \frac{1}{7}\sin 2\pi (7f_s)t + \text{-----} + \frac{1}{n}\sin 2\pi (nf_s)t)$$

$$BW \cong F_{Hi} = \frac{0.35}{t_r}$$

$$\%tilt = p\% = \frac{V - V^1}{V} \times 100\%$$

$$tilt = p = \frac{V - V^1}{V}$$

The low cutoff frequency is then determined from , $f_{L0} = \frac{P}{\pi} f_s$

Procedure:

1. Connect a square wave I/P from F.G b/w prints P1 & P2.
2. Connect a CRO b/w O/P terminals P3 & P4.
3. Adjust the frequency of the square wave such that the O/P waveform simulation of the waveform which is shown in the figure.
4. Calculate the value of raising time (t_r) V &V^1.
5. Calculate the lower &Upper cutoff frequency using the formula given above.
6. Verify the lower & upper cutoff frequency using sinewave signal.

Tabulation:

Sl No.	tilt	f_{Hi}	F_{L0}	P

Result:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

Viva Question

1.What is square wave testing?

2.What is square wave generator?

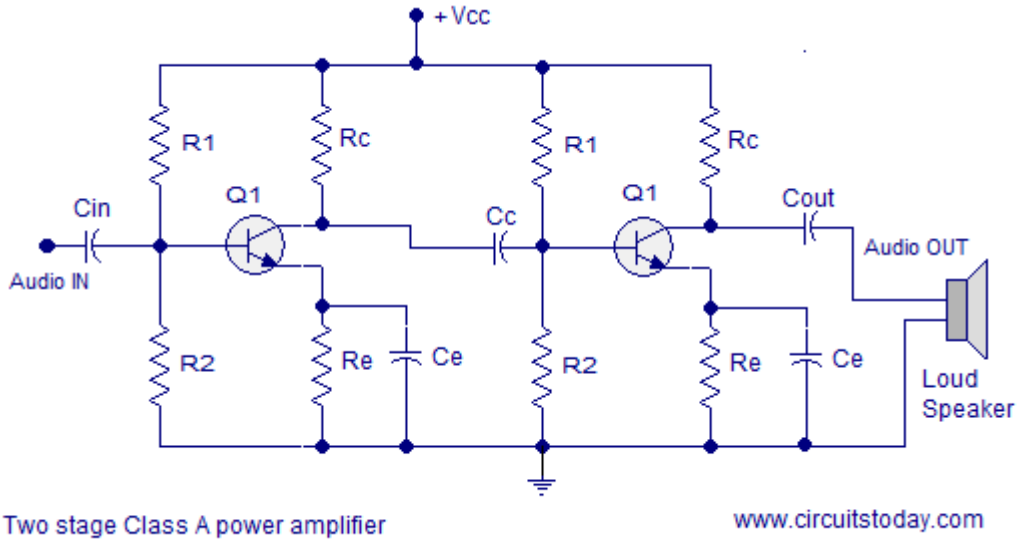
3.Why square wave is fed to an amplifier?

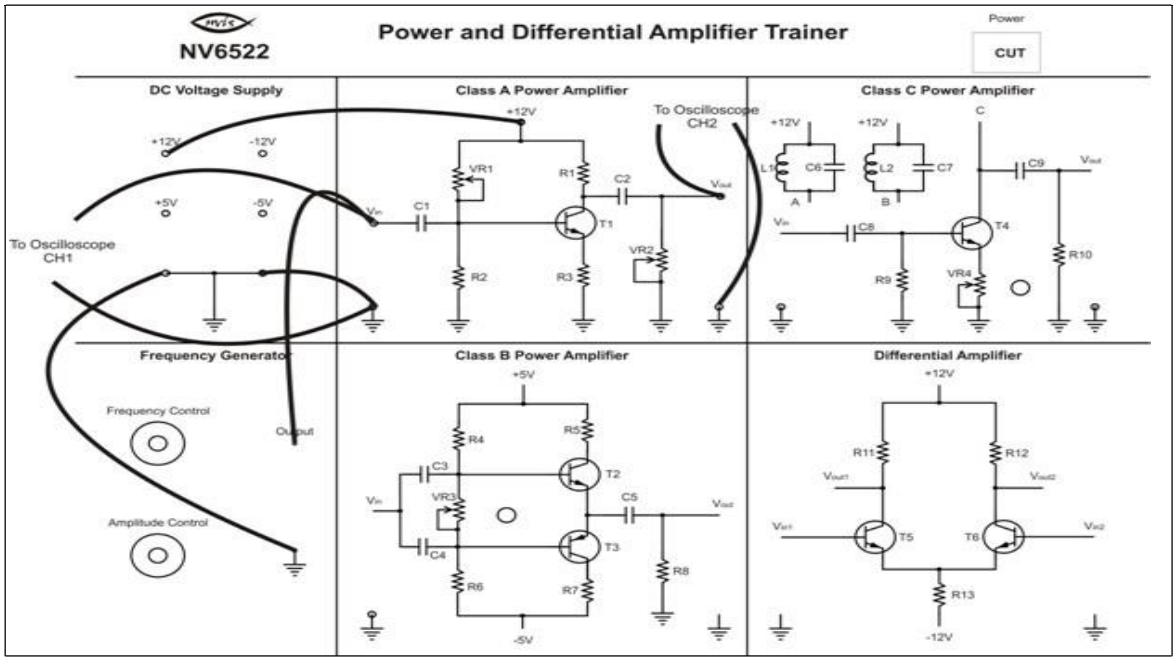
EXPT NO.-12
Class -A & Class-B power amplifiers.

Aim Of The Experiment:
To study the operation of Class 'A' Amplifier.

Apparatus Required:
1. Oscilloscope
2. Patch Cords

Circuit Diagram:
Circuit used to show the Class 'A' Amplifier operation is as shown below.





Theory:

The power amplifiers are the amplifiers which deliver maximum undistorted symmetrical output voltage swing to the low impedance load. Generally any system (like a stereo, radio or television) consists of several stages of amplification. When the signal passes through these stages, the power level of signal rises so much that the later stages require high power handling circuit elements such as power transistors. Also as the load impedance of these later stages is very small (of the order of 8 ohm for stereo amplifier speakers), heavy collector current flows. To handle this, transistors having power rating of 1W or more are used in power amplifiers.

Power amplifiers are broadly classified as:

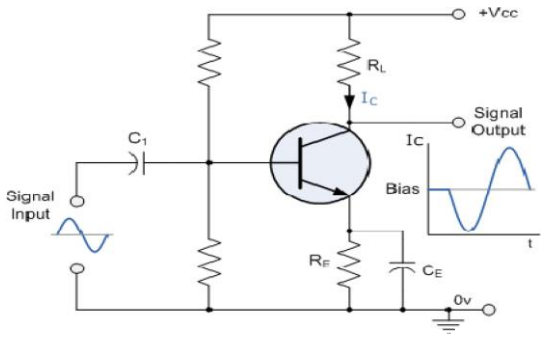
- Class A (VoltageAmplifier)
- Class B (Push-Pull EmitterFollower)
- ClassC

Class ‘A’ Amplifier:

The Class ‘A’ amplifier is the most common and simplest form of power amplifier that uses the switching transistor in the standard common emitter circuit configuration. The transistor is always biased "ON" so that it conducts during one complete cycle of the input signal waveform producing minimum distortion and maximum amplitude to the output. This means that the Class ‘A’ Amplifier configuration operates in the ideal operating mode, because there can be no crossover or switch-off distortion to the output waveform even during the negative half of the cycle. Class ‘A’ power amplifier output stages may

use a single power transistor or pair of transistors connected together to share the high load current.

Consider the Class 'A' amplifier circuit below:



This is the simplest type of **Class A** power amplifier circuit. It uses a single-ended transistor for its output stage with the resistive load connected directly to the collector terminal. When the transistor switches **"ON"** it sinks the output current through the collector resulting in an inevitable voltage drop across the emitter resistance thereby limiting the negative output capability. The efficiency of this type of circuit is very low (less than 30%) and delivers small power outputs for a large drain on the DC power supply. **Class 'A'amplifier** stage passes the load current even when no input signal is applied. So, large heat sinks are needed for the output transistors. However, another simple way to increase the current handling capacity of the circuit and obtain a greater power gain simultaneously is to replace the single output transistor with a **Darlington Transistor**. These types of devices comprises of basically two transistors within a single package, one small "pilot" transistor and another larger "switching" transistor. The big advantage of these devices is that the input impedance is suitably large while the output impedance is relatively low, thereby reducing the power loss and therefore the heat within the switching device.

Class 'A' Output Waveform:

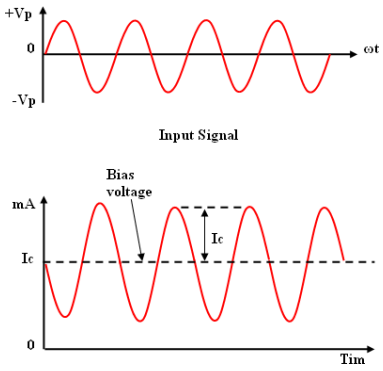


Figure 2

In this configuration, the Class A amplifier uses the same transistor for both halves of the output waveform and due to its biasing arrangement, the output transistor always has current flowing through it, even if there is no input signal. In other words the output transistor never turns **"OFF".** This results in very low efficiency as its conversion of the DC supply power to the AC signal power delivered to the load is usually very low. Generally, the output transistor of a Class A amplifier gets very hot even when there is no input signal present. So some form of heat sinking is required. The DC current flowing through the output transistor (Ic) when there is no output signal will be equal to the current flowing through the load.

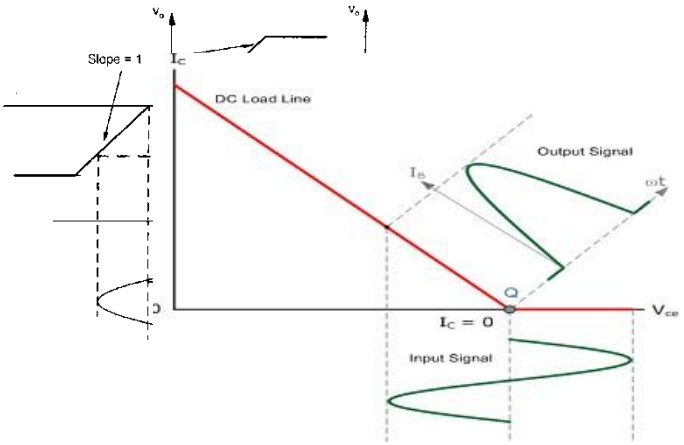
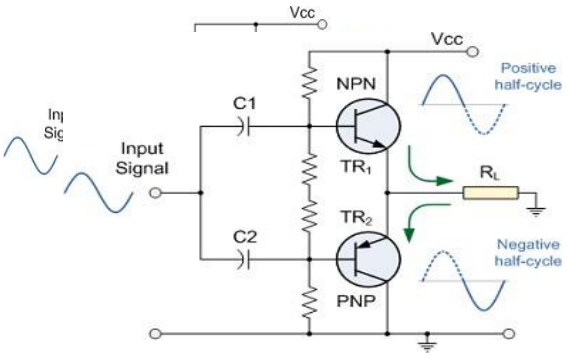


Figure 6



Procedure:

1. Connect the +12V DC supply to '**+12V'** of Class 'A' Amplifier and also '**Gnd**' to ground as shown in circuitdiagram.
2. Nowconnectthe"**Output**"ofFrequencyGeneratorto"**Vin**."ofClass'A'PowerAmplifierandas well as connect ground.
3. Connect CRO channel 1 to sockets '**Vin**' & '**Gnd**' of Class 'A' Power Amplifier using the CROprobe.
4. Set the VR1 and VR2 fully anticlockwisedirection.
5. Now switch On thesupply.

6. Using the '**Frequency Control'** and '**Amplitude Control'** knobs of the Function Generator, set the input signal at $2V_{p-p}$ Voltage, 10 KHzfrequency and observe it on Oscilloscope (channel 1).

   Note: Keep peak to peak voltage of input signal less than $4V_{pp}$ to avoid saturation of amplifier.

7. Connect CRO channel 2 to sockets '**Vout**' &'**Gnd**' of Class 'A' Power Amplifier using CROprobe.
8. Vary VR2 gradually towards clockwise direction up to the maximum amplification of the output signal isobtained.
9. Observe the amplified output on Oscilloscope (channel 2) with positiveclipping.
10. Now vary VR1 in clockwise direction, you will observe the +ve clipping disappears which shows that the Q-point is shifting below the DC load line (refer the theorysection).
11. Observe the amplified output on Oscilloscope (channel 2) which is 4Vpp approximately and also observe the phase shift of180°.

    Note: For observing I/P & O/P waveform simultaneously keep the Oscilloscope at **Dual** mode.

Observation

Sl. No.	**Amplitude of Input Signal (V_{IN})**	**Amplitude of Output Signal (V_{out})**	**Gain $A_V = V_{out}/V_{in}$**

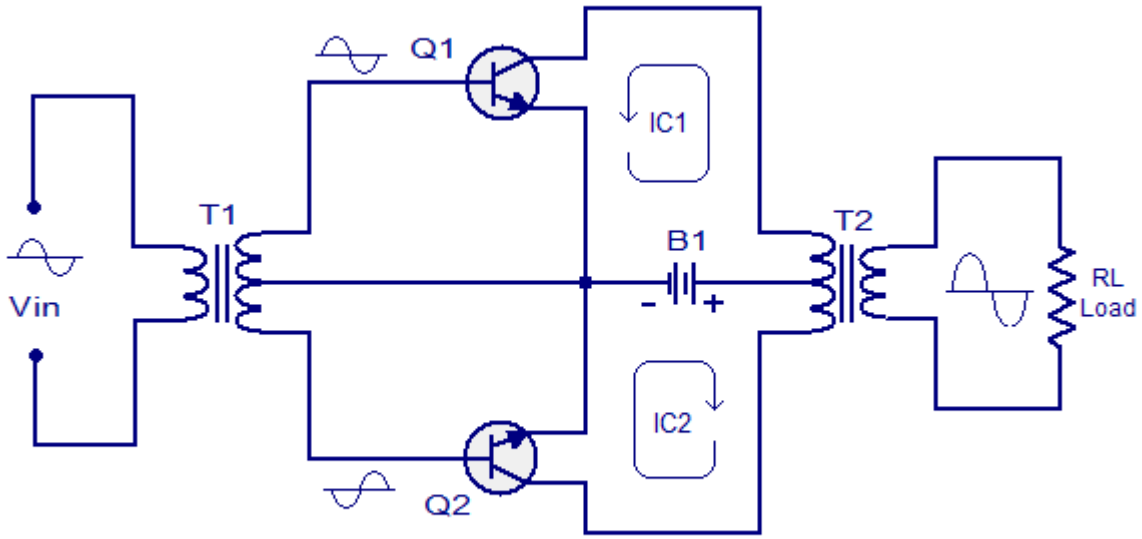
Objective:

To study the operation of **Class 'B'** Amplifier.

Apparatus Required:

1. Oscilloscope
2. Patch Cords

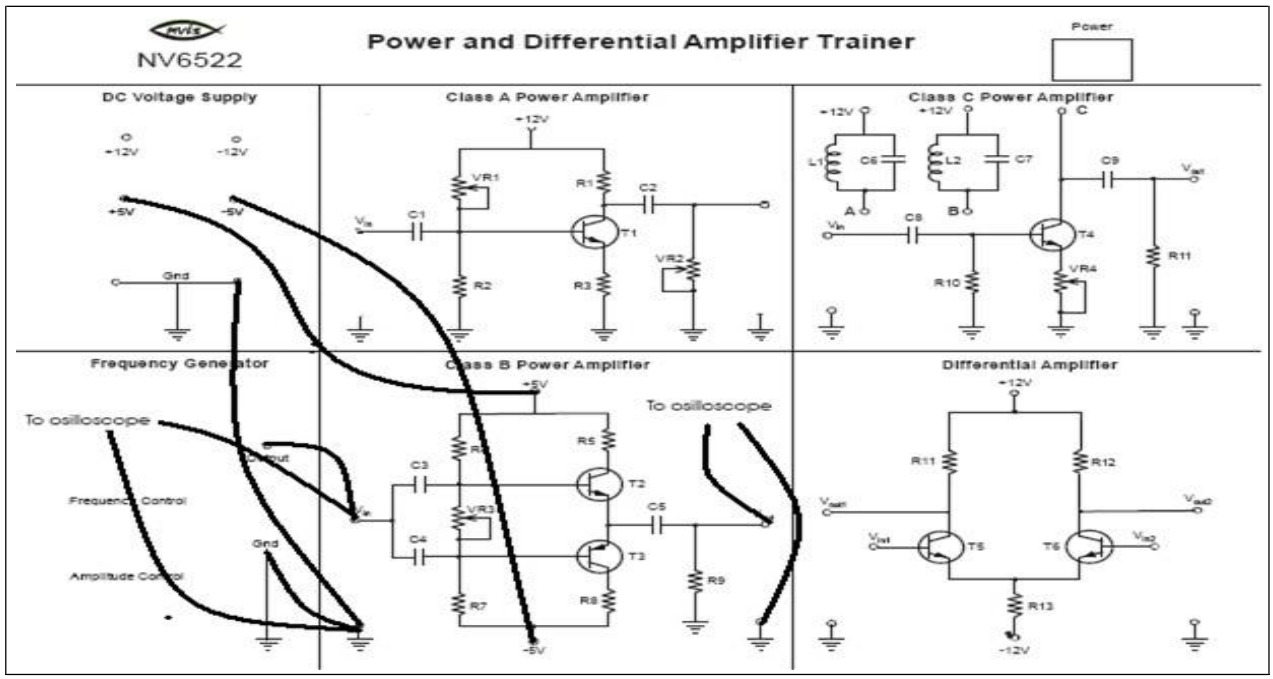
Circuit Diagram:



Transformer coupled Class B amplifier

www.circuitstoday.com

Circuit Diagram



Class 'B' Amplifier:

Class B amplifier is a circuit in which transistor conducts (collector current flows) for only 180 degree of input AC signal. When a signal is applied, one half cycles will forward bias the base-emitter junction and $I_C$willflow.Theotherhalfcyclewillreversebiasthebase-emitterjunctionand$I_C$willbecutoff.

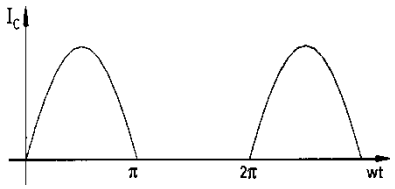


Figure 3

For **class B** amplifiers the Q point is located near the cutoff point of the AC load line. Thus, to amplify entire input AC signal a combination of two **class 'B'** amplifiers are used. One of which amplifies positive half cycle of input AC signal and the other amplifies negative half cycle of input AC signal. This amplifier configuration is known as push-pull or complementary symmetry. In the push-pull configuration it is important to match the two transistors carefully for the proper amplification of both the halves. While the input signal is being amplified through **class B** amplifier the input signal has to rise to about **0.7V** to overcome the barrier potential of amplifying transistor. During this period no current flows through the circuit and output is zero. The action is similar for both the transistors.

Thus, following characteristic is obtained for input and output voltages:

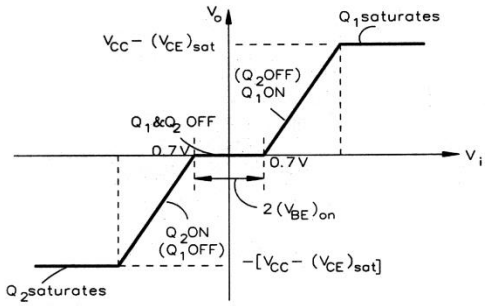


Figure4

The output signal no longer remains sine wave and gets distorted. Since the clipping occurs between the time when one transistor cuts off and the time the other becomes **ON**, we call it crossover distortion

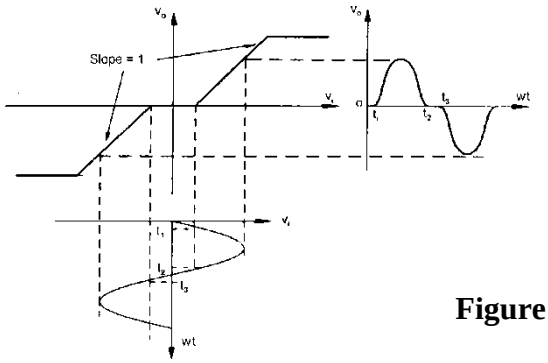


Figure 6

To remove the crossover distortion a slight forward bias is applied to each emitter diode i.e. we locate the Q point of both the transistors slightly above the cutoff. Thus collector current in both the transistors flows for more than 180° but less than 360°. Sometimes we call such an amplifier as **Class AB** amplifier.

Class B: Output Characteristics Curves:

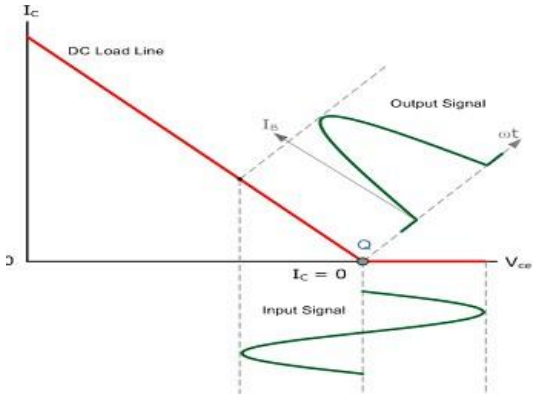


Figure 6

Class B Amplifiers have the advantage over their **Class A** amplifier cousins in that no current flows through the transistors when they are in their quiescent state (i.e. with no input signal), therefore no power is dissipated in the output transistors or transformer when there is no signal present unlike **Class A** amplifier stages that require significant base bias thereby dissipating lots of heat - even with no input signal. So the overall conversion efficiency (η) of the amplifier is greater than that of the equivalent Class A with efficiencies reaching as high as **75%** possible resulting in nearly all modern types of push-pull amplifiers operated in this **Class B** mode.

Procedure:

1. Connect**+5V**and-**5V**DCpowersuppliesattheirindicatedpositionfromDCVoltageSupplyto Class 'B' Power Amplifier & also '**Gnd**' to ground.
2. Now connect the "**Output**" of Frequency Generator to "**Vin**." of Class 'B' PowerAmplifier and as well as connect ground.
3. ConnectCROchannel1tosockets'**Vin**'and'**Gnd**'ofClass'B'PowerAmplifierusingtheCR O probe.
4. Put the VR3 to its minimum position i.e. rotate it fully anticlockwise. (This is the condition when no bias voltage is applied to the emitter diodes of both thetransistors.)
5. Now switch On thesupply.
6. Using the '**Frequency Control'** and '**Amplitude Control'** knobs of the Function Generator, set the input signal at $2V_{pp}$ Voltage, 10 KHzfrequency and observe it on Oscilloscope (channel 1).
7. Connect Oscilloscope (channel 2) at the '**Vout'** and '**Gnd'** terminals of Class 'B'

Power Amplifier and observe the output waveform. The crossover distortion can be clearly observed on the oscilloscope.

Note: For observing I/P & O/P waveform simultaneously keep the Oscilloscope at **Dual** mode.

8. Gradually increase the bias voltage by increasing bias resistance VR3 (i.e. rotate the VR3 in clockwise direction) up to the value when the crossover distortion is completely removed and maximum amplification of the input signal isobtained.

9.Now observe the amplitude of input & output signal and calculate the voltage gain. (The class B amplifier has unity voltagegain).

Observation

Sl. No.	**Amplitude of Input Signal (V_{IN})**	**Amplitude of Output Signal (V_{out})**	**Gain $A_V = V_{out}/V_{in}$**

Results:

Conclusion:

PRECAUTION:

1. All connections should be right and tight.

2. Do not touch any live terminal.

3. Power must be switched off whenever an experiment or project is being assembled or disassembled.

VIVA QUESTIONS:

1. What is meant by conversion efficiency? Which type of power amplifier has the maximum conversion efficiency? Why?

2. To which class does the push-pull amplifier belongs and what are the advantages of it?

3. What is meant by crossover distortion? In which power amplifier it is maximum?

4. Why class-A amplifier is used in transmitter modulators?

5. What is the maximum theoretical efficiency of a class-A amplifier?

6. Which harmonics are eliminated in the class –B push-pull amplifier?

7. What is meant by complementary symmetry push-pull amplifier? State its advantages.

8. Why the load is to be coupled through a transformer in a class-A amplifier?

9. Discuss the stability techniques of power amplifier?

10. Draw the thermal equivalent circuit of a power amplifier?