Date: 13/08/2019

Father of Electrical Engineering → William Gilbert

Vaccum 1905

PN J/A Deade 1939 Invented by. Shockley

Transistor 1947

J Bardeen, W H Brattain and W Shockley

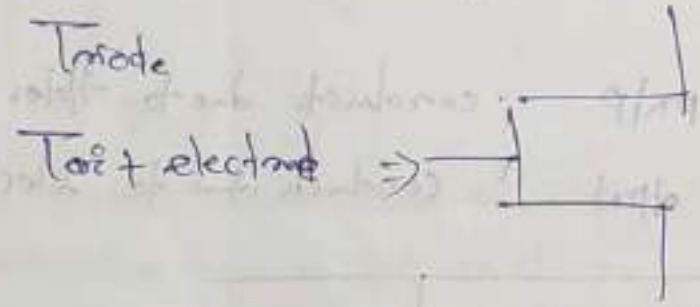
Russel

1956 ⇒ Noble Prize. → 1972

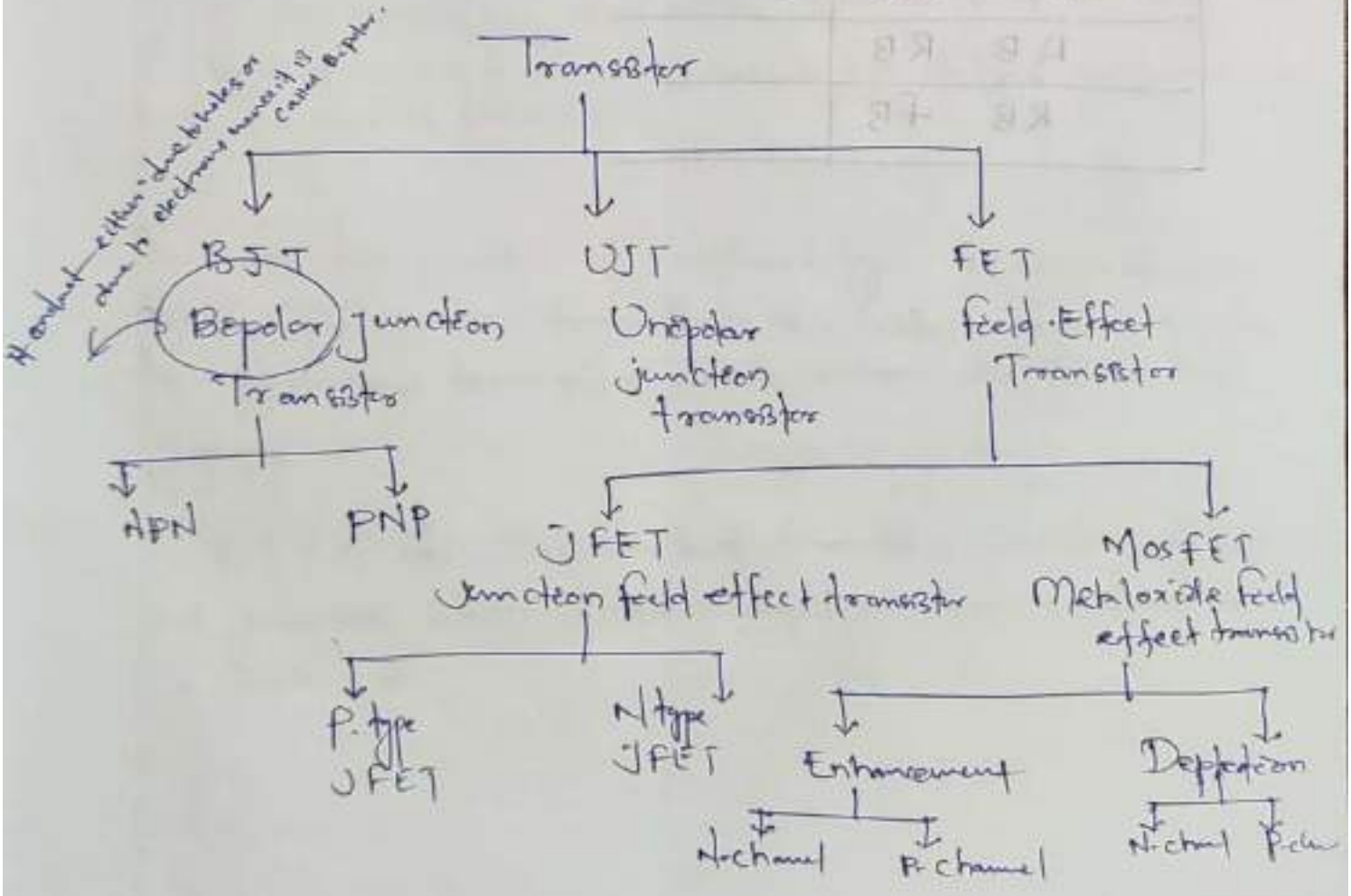
famous Scientist in Electronics

Vaccum Tube Triode

Tri + electrode ⇒



Transistor (Transfer + Resistor) ← Jhon R. Pierce



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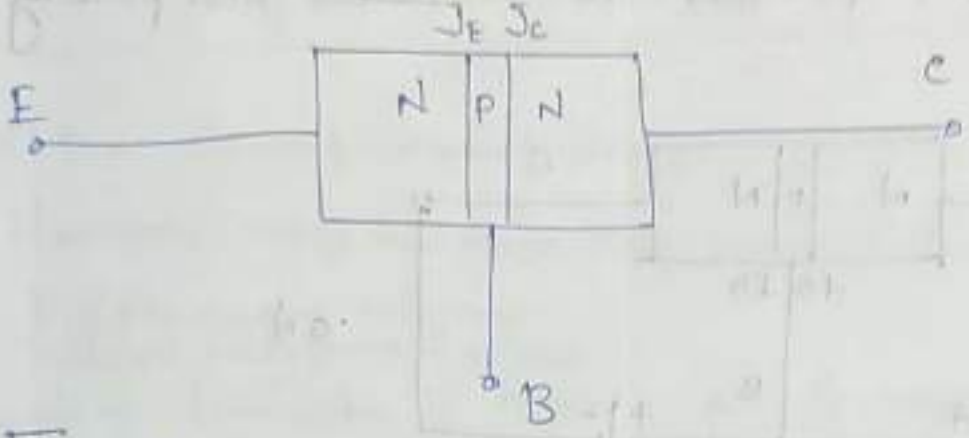
TRANSISTOR

Date: 17/09/19

The word derived from transfer + Resistor

It is a 3 terminal 3 layer device (NPN, PNP)

Emitter, Base, Collector.



For formation of transistor, any one of semiconductor is sandwiched between other type of semiconductor.

for examples: An N-type can be sandwiched between two P-type semiconductors that will be form a PNP similarly, one P-type can be sandwiched between two N-type semiconductor to form a N-P-N transistor.

There are two junctions of a different types of semiconductors this is called junction transistor. It is called bipolar because the conduction takes place due to electrons as well as holes.

BJT:

BJT is the Basic model of transistor. Consisting of two PN junction. which is able to amplify a signal or works as a switch.

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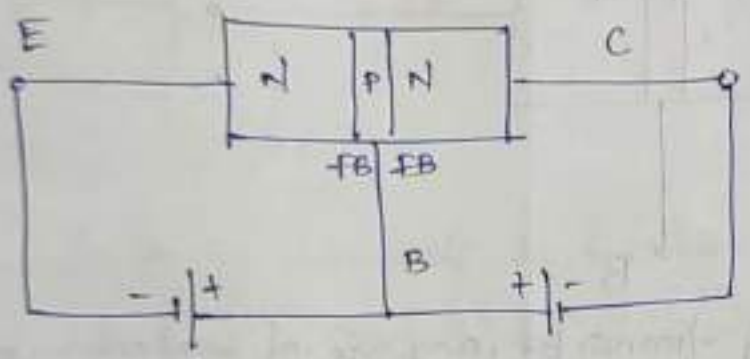
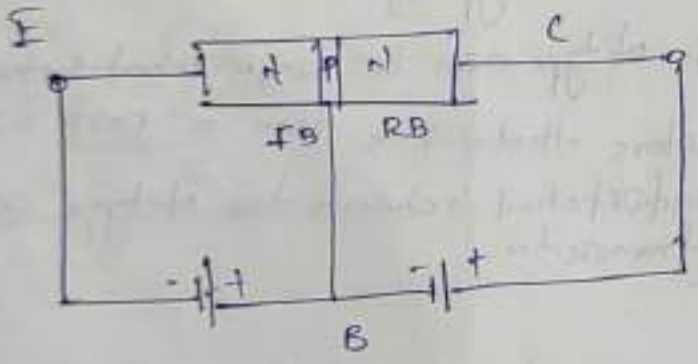
Transistor Action:

Transistor of both types (PNP & NPN) behave exactly same way, except change in majority carriers

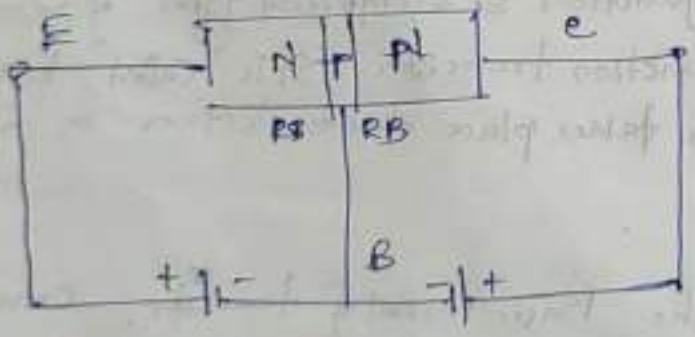
* In PNP transistor the conduction takes place by holes
* In NPN transistor the conduction takes place by electrons



ON



Amplifier



off

Region of Operation:

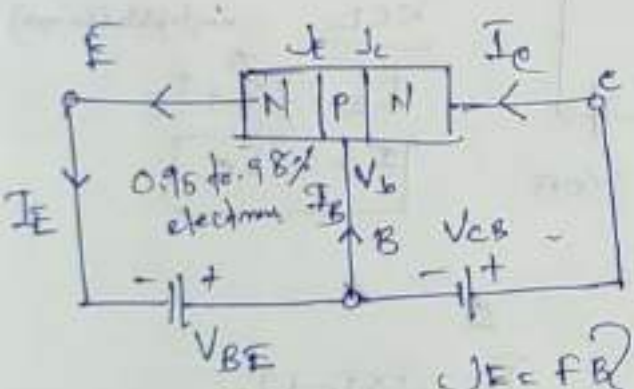
J_E	J_C	Operating region	Application
FB	RB	⇒ Active Region	⇒ Amplifier
FB	FB	⇒ Saturation Region	⇒ "ON" switch
RB	RB	⇒ Cutoff Region	⇒ "OFF" switch
RB	FB	⇒ Inverting mode	⇒ rarely used.

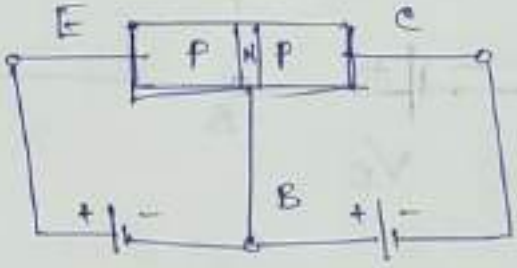
→ It is a Current control device.

→ However, NPN transistor are prefered due to a better high frequency response.

→ NPN transistor is better, as it response high frequency response.

Working of transistor:





J_E = FB, J_C = RB } Active

V_{BE} (not V_{EB}) :⇒ Because higher potential is connected to Emitter side.

Breakdown does not happen in transistor.

V_b at J/N J_E ⇒ $V_b = V_{BE} - V_b$

V_b is the barrier Potential. V_b at J/N J_1 = $V_{BE} - V_b$

V_b at J/N J_2 = $V_{CB} + V_b$

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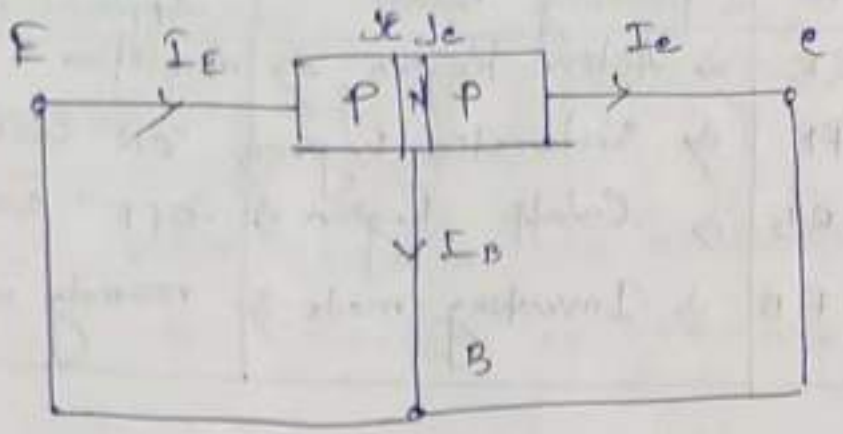

JE = FB
JC = RB

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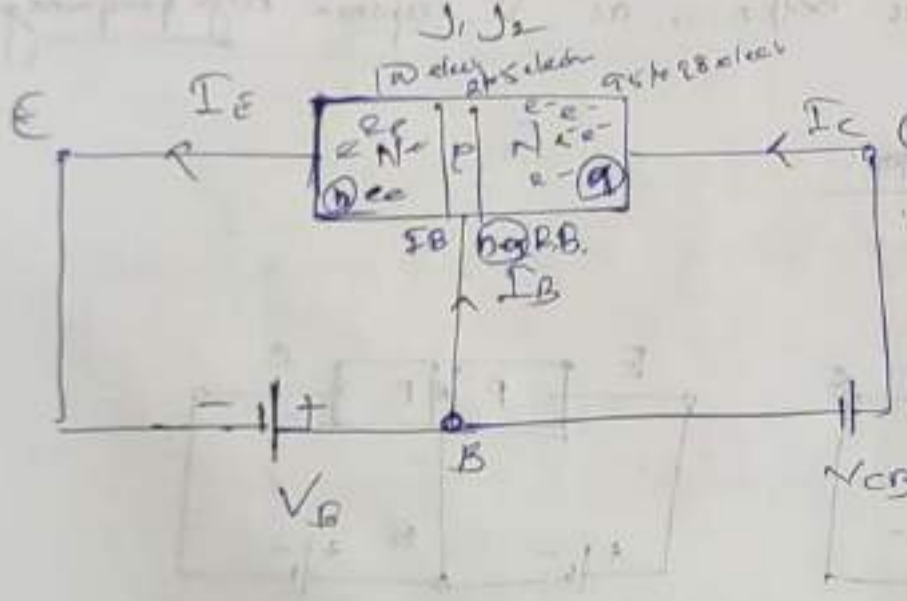


KCL, neglected (as very)

$I_E = \cancel{I_B} + I_C$

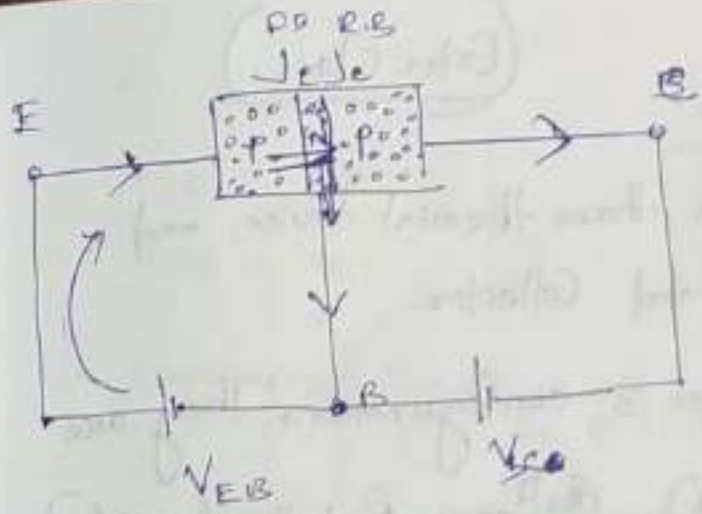
$I_E = I_C$

②

$I_E = \alpha I_C + I_{CO}$

Here, In N-transistor, two junctions and J_1 and J_2 and Base is common to both the the Emitter and Collector.

The J_1 is FB and J_2 is RB. J_1 of N terminal is connected to the -ve terminal of the battery and hence the majority charge carriers of the N type electrons and repels and moves towards the P-region and some of the electrons and combine with some holes and after breaking potential barrier they moves towards N region. because J_2 N region is connected to the terminal which attracts the electrons. Here 'P' terminal is



$$I_E = I_B + I_C$$

$$I_E = I_C + I_{CO}$$

con

(Extra Class)

Configuration of transistor:

The transistor is a three terminal device and they are emitter, base and collector.

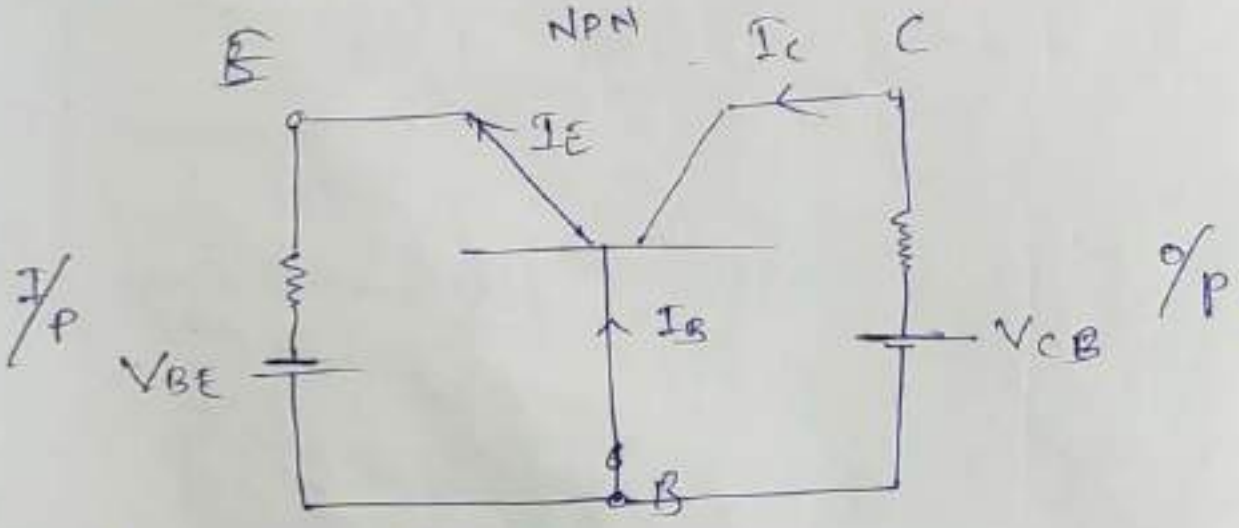
because of this there are 3 configurations. They are

(1) Common base (CB) (Base common for both i/p & o/p)

(2) Common Emitter (CE) (Emitter common ..)

(3) Common Colector (cc) (Collector ..)

Common Base:



Active mode Operation:

J_1 - FB

J_2 - RB

Diode ⇒ Single - VI characteristics

Transistor ⇒ Two port - I/p & O/p

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Assume,

$V_{BE} = V_{EE}$

$V_{CB} = V_{cc}$

Applying KCL,

$I_E = I_C + I_B$ ($I_B \to 0$)

~~or $I_C = \alpha I_E + I_{CBO}$~~

or $\alpha I_E = I_C - I_{CO}$

$I_C = \alpha I_E + I_{CBO}$ ($I_{CBO} \to 0$)

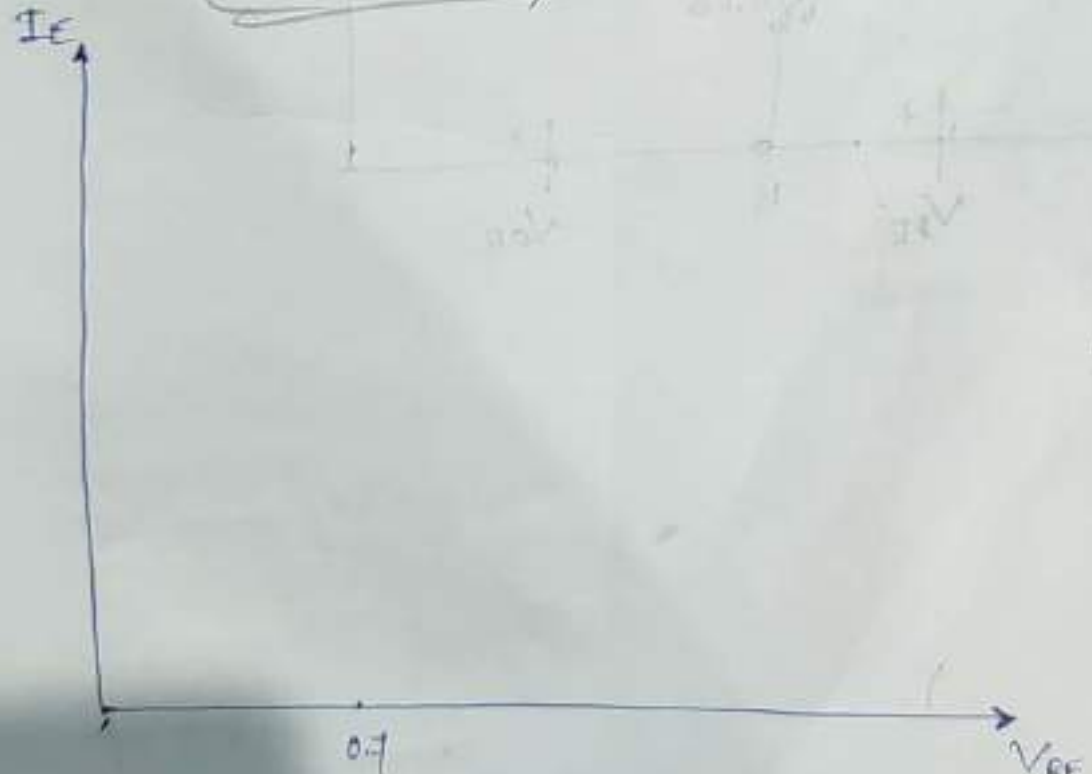
$I_E \gg I_{CBO}$

$I_C = \alpha I_E$

$$\boxed{\alpha = \frac{I_C}{I_E}} = \frac{\text{O/p curt}}{\text{I/p curt}}$$

α = Common base current gain.

α = 0.95 to 0.98 %



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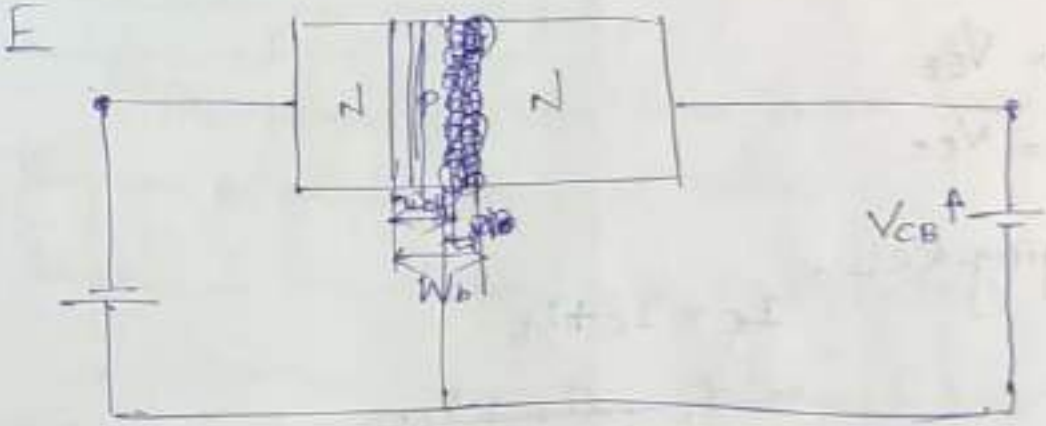


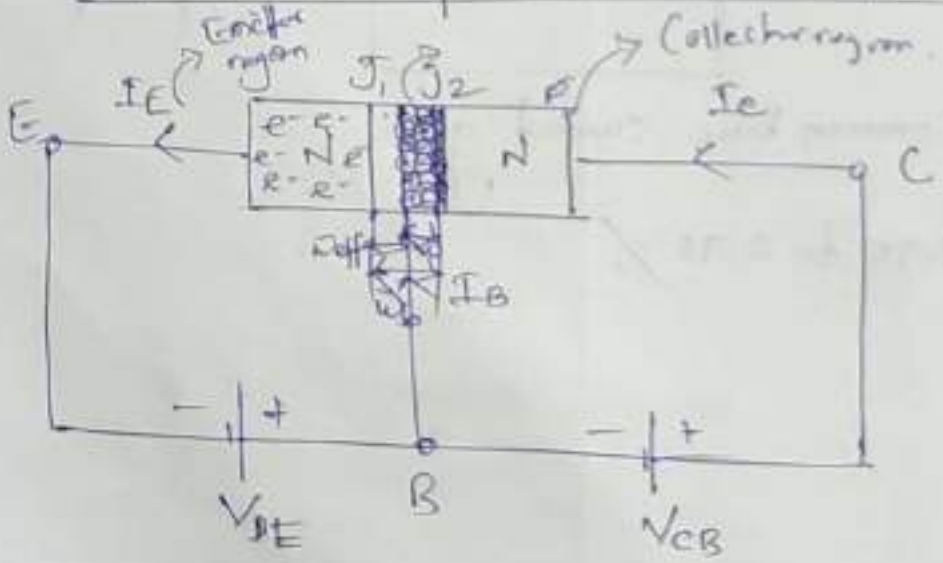
$W_b = W_{eff} + W$

$W_{eff} = W_b - W$

$V_{CB} \uparrow \Rightarrow W \uparrow \Rightarrow W_{eff} \downarrow$ ($I_c \uparrow$)

Date: 21/09/19

Input and Output Characteristics of CB configuration



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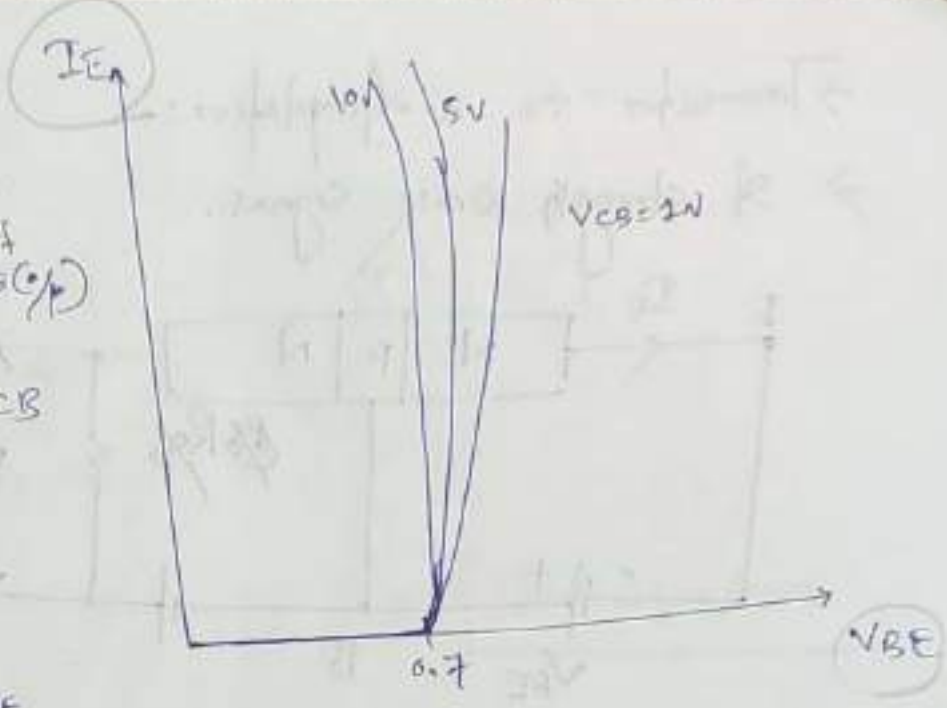
Input characteristics

$I_{I/P}$ $V_{I/P}$: different values of V_{CB} (O/P)

$I_{I/P} \Downarrow I_E$

$V_{I/P} \Downarrow V_{BE}$

V_{CB} (O/P) $\Downarrow V_{CB}$



$I_C = \alpha I_E$

$\omega_B =$

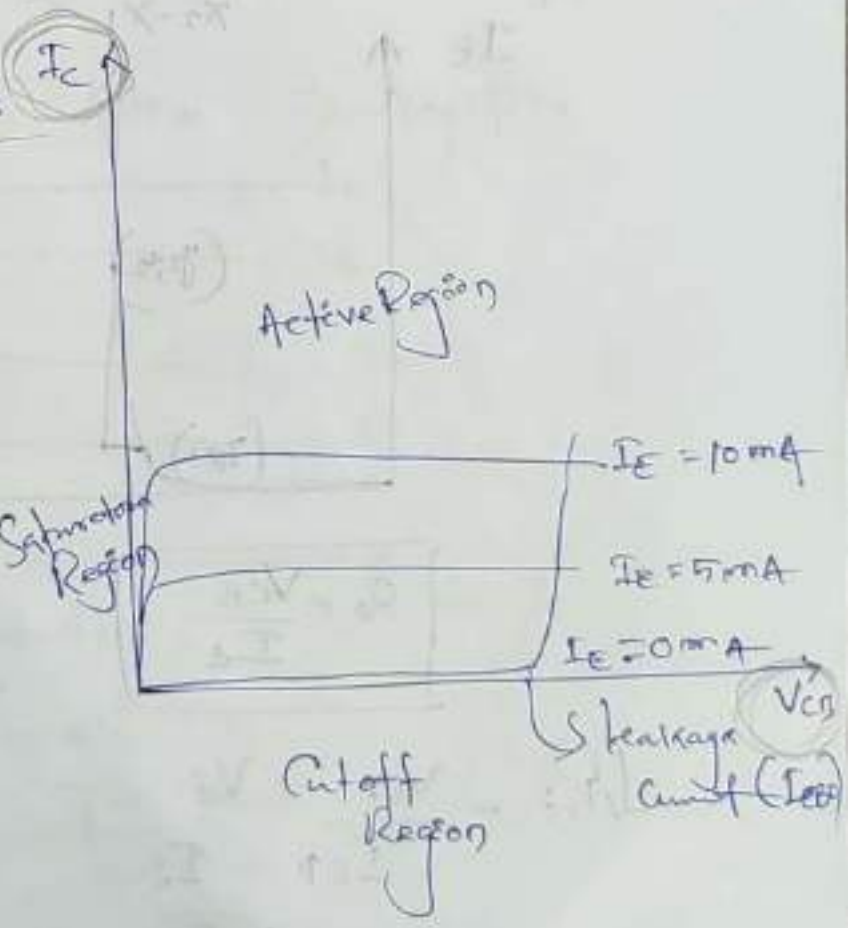
Output characteristics

$I_{C/P}$ $V_{C/P}$ I_C ($I_{B/P}$)

$I_{C/P} \Downarrow I_C$

$V_{C/P} \Downarrow V_{CB}$

I_C ($I_{B/P}$) $\Downarrow I_E$



$I_C = \alpha I_E$

α (0.95 to 0.98)

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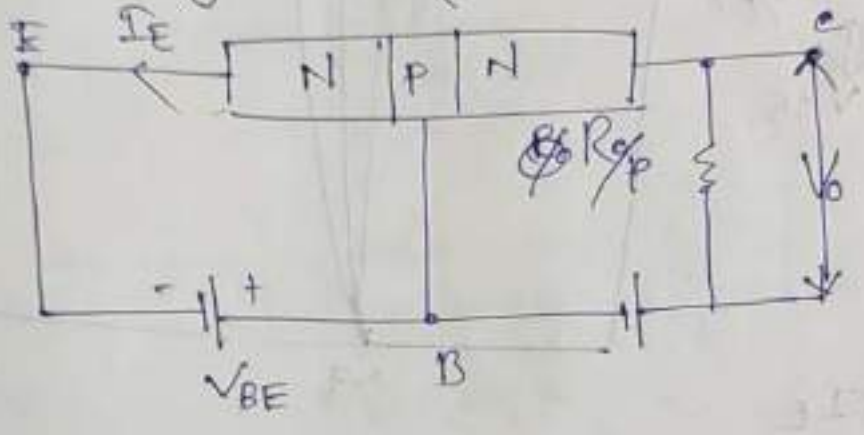
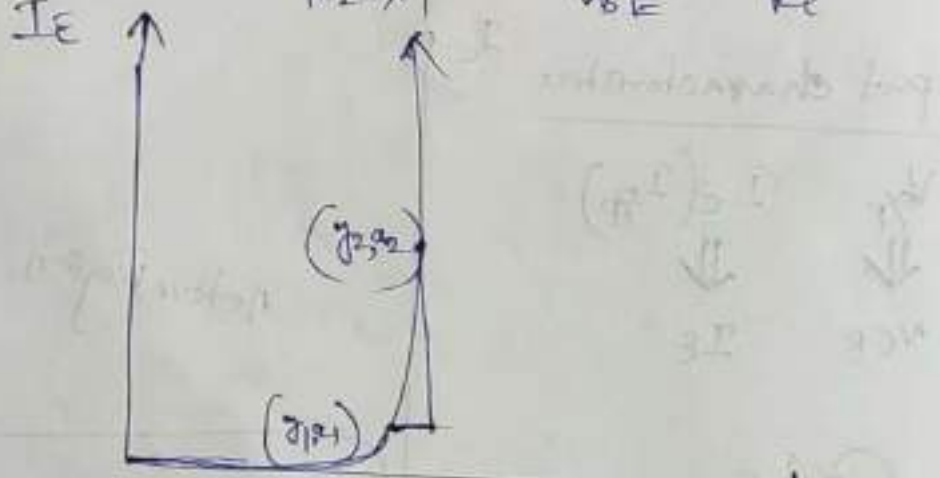
→ Transistor is a Amplifier:

→ a strength weak signal.



slope, $m = \frac{y_2 - y_1}{x_2 - x_1} = \frac{I_E}{V_{BE}} = \frac{1}{R_i}$



$$R_o = \frac{V_{CB}}{I_e}$$

$$R_i = \frac{V_{BE}}{I_E} = \frac{V_i}{I_i}$$

$$V_i = I_i R_i$$

$$V_i = I_E R_i$$

$$I_E = \frac{V_i}{R_i} = \frac{20mV}{20\Omega} = 1mA$$

$$I_C = \alpha I_E$$

$I_C \simeq I_E$ (0.95 - 0.98 α)

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$\Rightarrow I_C \simeq 10\,mA$

$V_o = R_{\text{eq}} I_e$

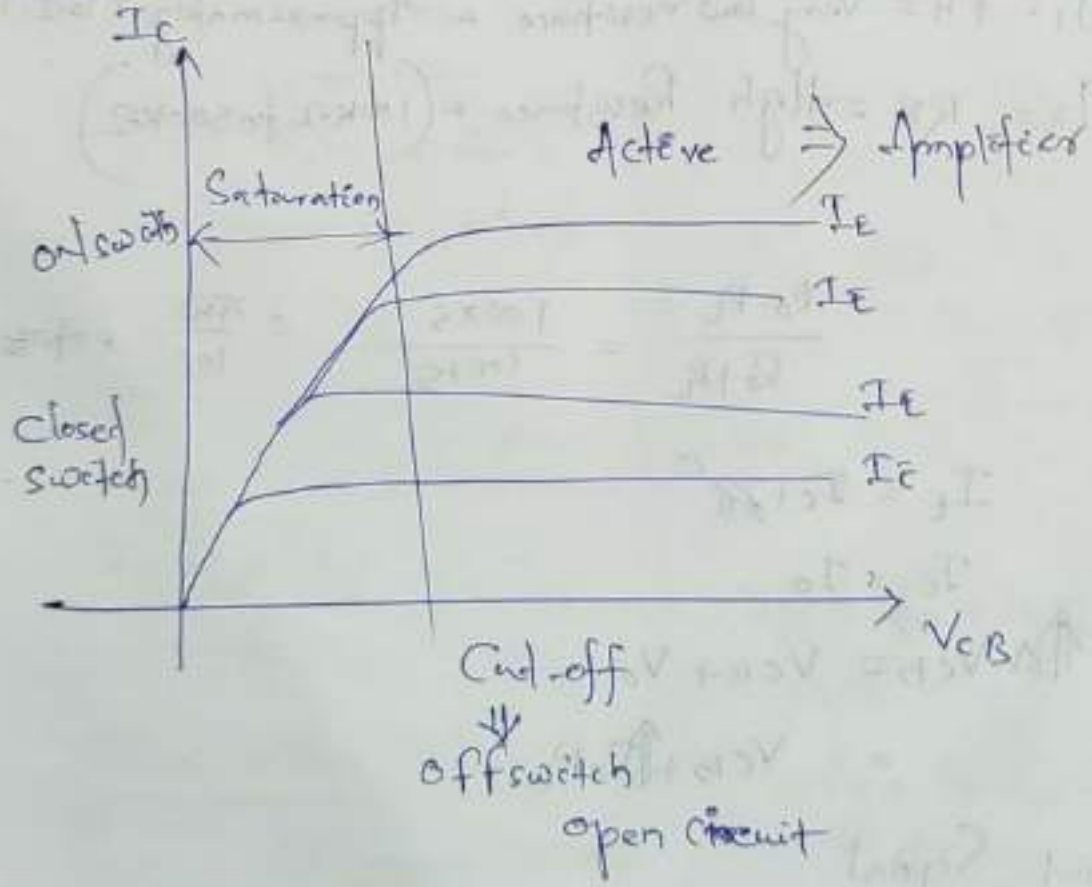
$V_o = (R_L + R_e)\,10mA$

$= (20+5)\,10mA$

$V_o = (25)(10mA)$

Date: 24/09/2019

From the output:



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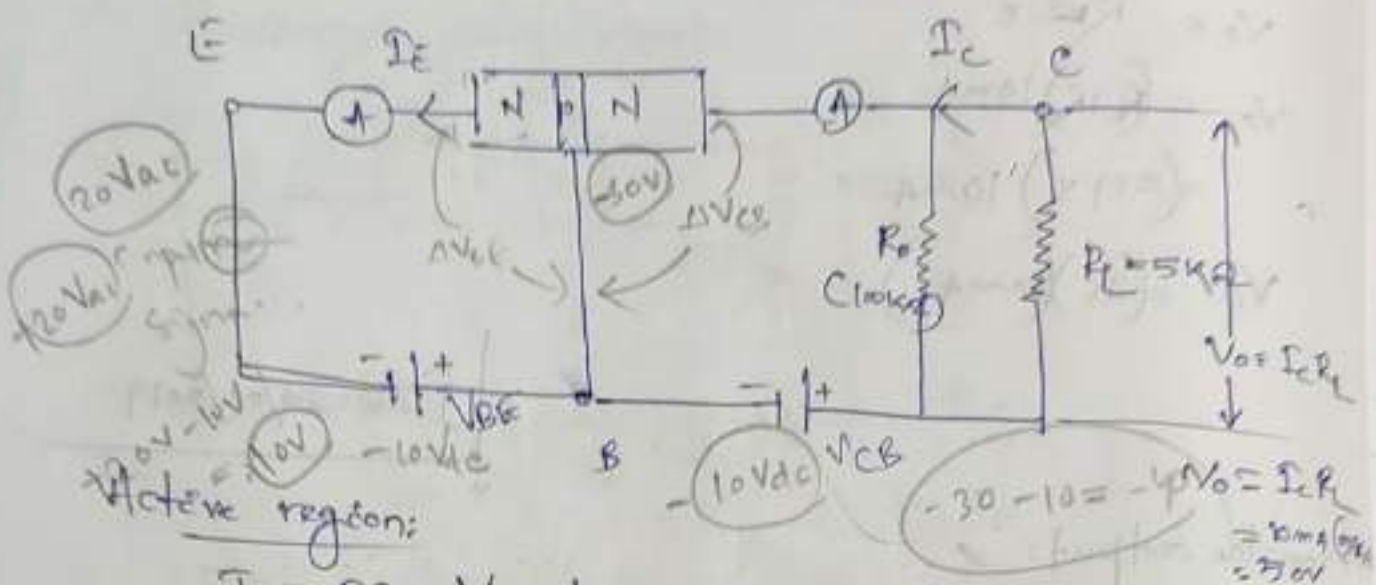
Transistor as Amplifier:



Active region:

J_1 = FB = Very low resistance = Approximately (10Ω-10Ω)

J_2 = RB = High Resistance = (100kΩ to 500kΩ)

$$\frac{R_o - R_L}{R_o + R_L} = \frac{100 \times 5}{100 + 5} = \frac{500}{105} = 4.76$$

$I_E = I_C + I_B$ (0)

$I_E = I_C$

$\Delta V_{CB} = V_{CB} + V_o$

$= V_{CB} + \Delta I_C R_L$

Input Signal

+ve half	-ve half
$(+V_e ac) + (-V_e dc)$	$(-V_e ac) + (-V_e dc)$
FB ↓ I_E ↓ I_C ↓	More FB ↑ I_E ↑ I_C ↑
ΔV_{CB} ↓	ΔV_{CB} ↑
$-V_{CB}$ ↑	$-V_{CB}$ ↑

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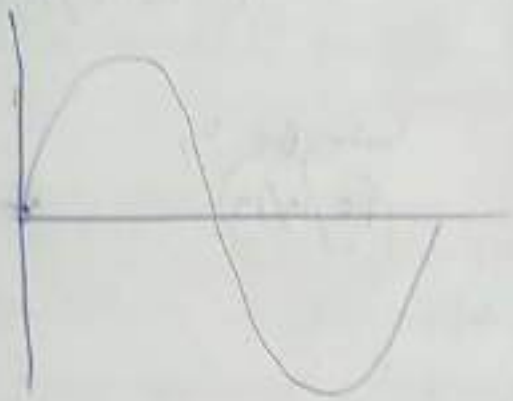
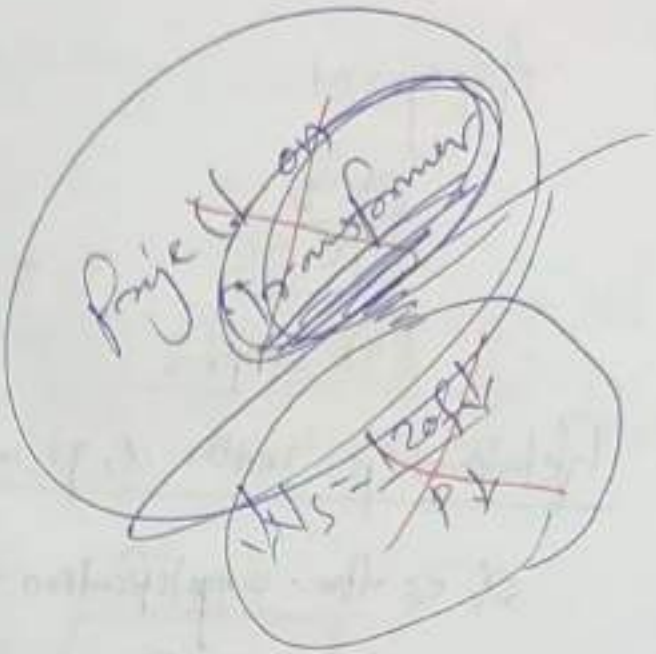




$+20V - 10V = +10V$

$R_L = 20\Omega$

$I_c = \frac{V}{R} = \frac{10}{100} = 0.5A$

$I_c = 0.5A$

$R_0 = 100\Omega$

$\Delta V_{CB} = V_0 + V_{CB}$

$R_0 = \frac{V_{CB}}{I_c}$

$\frac{10}{0.5} = 20$

$R_0 = 1\Omega$ KΩ

$\Delta V_{CB} = R_0 I_c$

$\Delta V_{CB} = 30 + V_{CB}$

$I_E = I_B + I_C$

$I_E = I_C$

$\Delta V_{BC} = V_{BE} - I_C R_L$

$V_{BC} = V_{BE} + I_C R_L$

$\Delta V_{BC} = 30$

$\Delta V_{BC} = V_{BC} - I_C R_L$

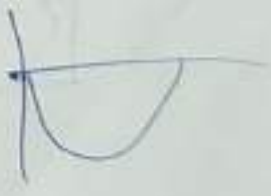
$10 = 20 - 15$

5

Input Signal

during Input Signal.

+Ve half cycle	during -ve half cycle
(+Ve ac) + (+Ve dc)	(-Ve ac) + (+Ve dc)
FB ↑ I_B ↑ I_E ↑ I_C ↑	FB ↓ I_E ↓ I_C ↓
ΔV_{BE} ↑	ΔV_{BE} ↑
	-Ve ↑



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Date: 15/10/19

Assignment.

Submitted by
10/10/19

(i) CE
(ii) CC
(iii) Clampers

Relationship betn α, β and γ:

α is the amplification factor in Common base configuration

$$\alpha = \frac{I_C}{I_E} = \frac{\text{O/P Current}}{\text{I/P Current.}}$$

β is the amplification factor in Common emitter Configuration

$$\beta = \frac{I_C}{I_B}$$

γ is the amplification factor in Common Collector.

$$\gamma = \frac{I_E}{I_B}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\gamma = \beta + 1$$

$$\gamma = \frac{\alpha}{1-\alpha} + 1$$

$$\gamma = \frac{\alpha + 1 - \alpha}{1-\alpha} = \frac{1}{1-\alpha}$$

$$\gamma = \frac{1}{1-\alpha}$$

or, $$\gamma = \beta + 1 = \frac{1}{1-\alpha}$$

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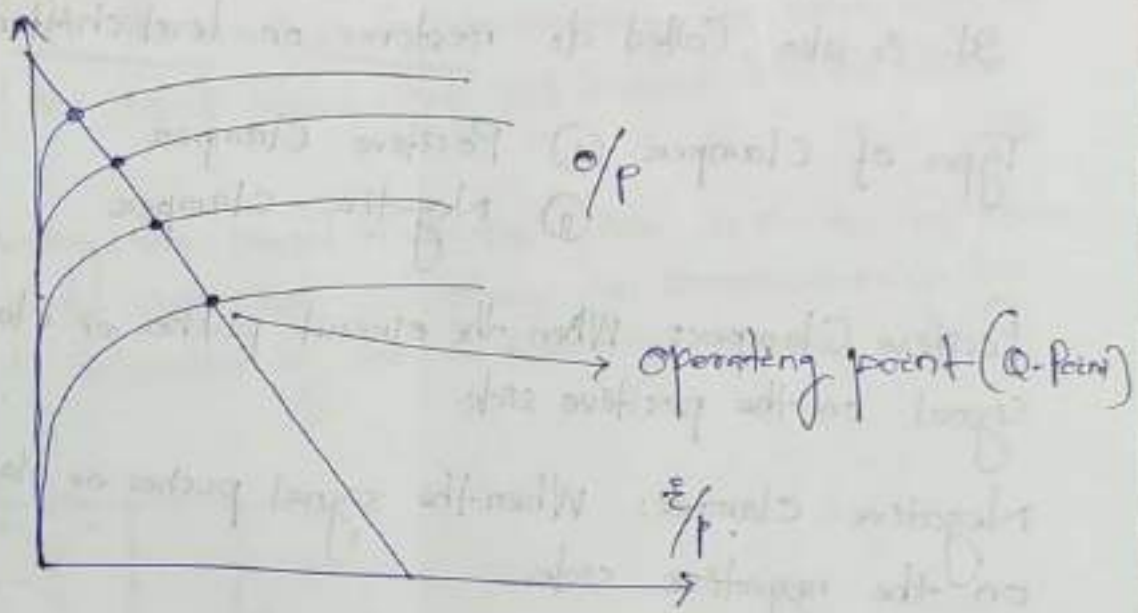
Transistor load line analysis: (operating point & Biasing)

Transistor load line analysis: → DC load line analysis
→ AC load line analysis

* DC load line analysis:

The DLL is defined as the, locus of operating point on the o/p characteristics of the transistor. It is the line on which the operating point moves when ac signal is applied to the transistor.



* DC load line analysis:

The method for finding out I_C (output Current) values for different values of V_{CE} in absence of ac signal

Assignment: Date: 15/10/19

-:CLAMPERS:-

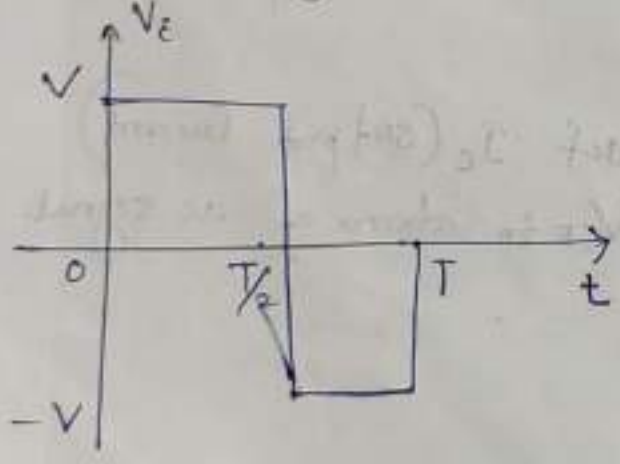
Defn: A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

It is also Called dc restorer or level shifter.

Types of Clampers (i) Positive Clamper
(ii) Negative Clamper

Positive Clamper: When the circuit pushes or clamps the signal on the positive side.

Negative clamper: When the signal pushes or clamps the signal on the negative side.



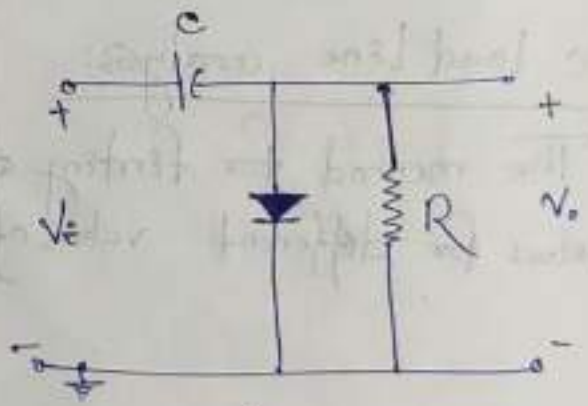


fig. 1

Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

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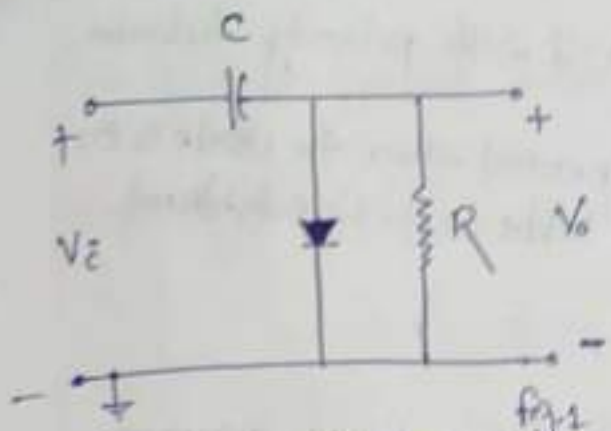

fig.1

clamper

Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.

Step 2: During the period that the diode is in the 'on' state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.

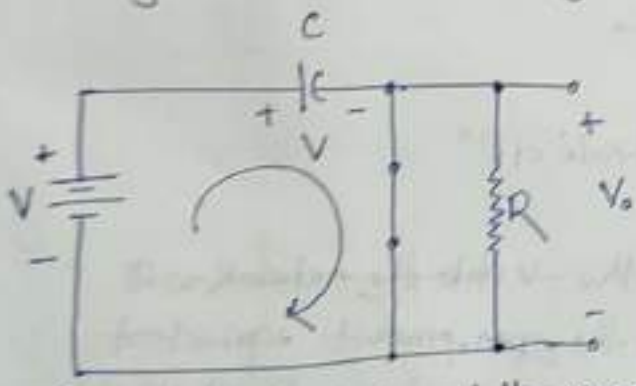

fig.2: Diode "on" and the capacitor charging to V volts.

For the network of fig.1 diode will be forward biased for the positive portion of the applied signal. For the interval of 0 to T/2 the network will appear as shown in fig.2.

The short-circuit equivalent for the diode will result in $V_o = 0V$ for this time interval as shown in fig.4. During the same interval of time, the time constant determined by $\tau = R_f C$ is very small because the resistor R has been effectively "shorted out" by the conducting diode and only resistance present is the internal (contact, wire) resistance of the network. The result is that the capacitor will quickly charge to the peak

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value of V volts as shown in fig. 2. with polarity indicated.

Step 3: Assume that during the period when the diode is in the "off" state the capacitor holds on to its established voltage level.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for v_o to ensure that the proper levels are obtained.

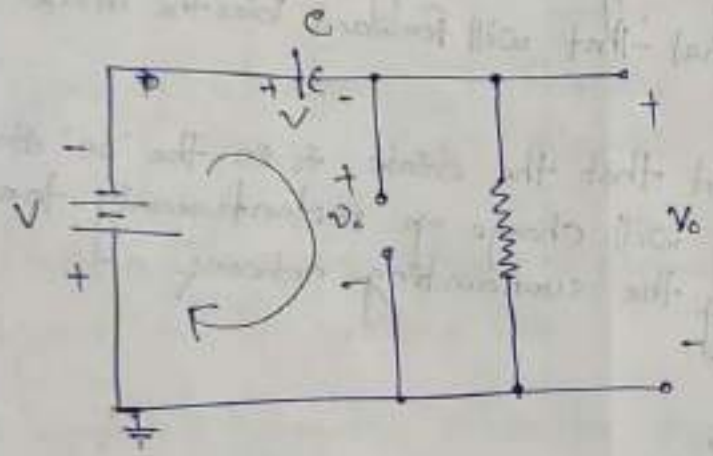

fig. 3: Determining V_o with the diode "off"

When the input switches to the -V state the network will appear as shown in fig. 3 with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor - both "pressuring" current through the diode from cathode to anode. Now that R is back in network the time constant determined by the RC product is sufficiently large to establish a discharge period so much greater than period $T/2 \rightarrow T$, and v_c can be assumed on an approximate basis that capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

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Since v_o is in parallel with the diode and resistor.

Applying KVL around the input loop in fig. 3.

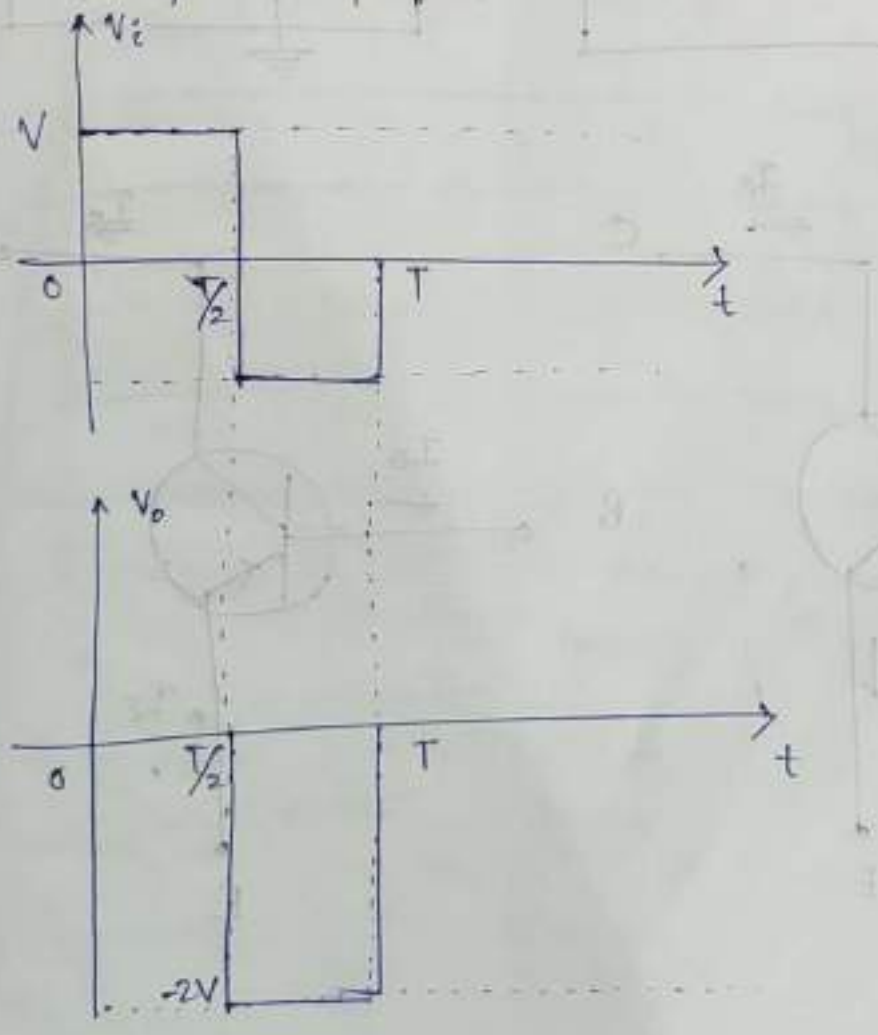
$$-V - V - V_o = 0$$

and $$V_o = -2V$$

The negative sign results from the fact that the polarity of 2V is opposite to the polarity defined for V_o. The resulting output waveform appears in fig.4 with the input signal.

The output signal is clamped to 0V for the interval 0 to T/2 but maintains the same total swing (2V) as the input.

Steps: Check that the total swing of the output matches that of the input.



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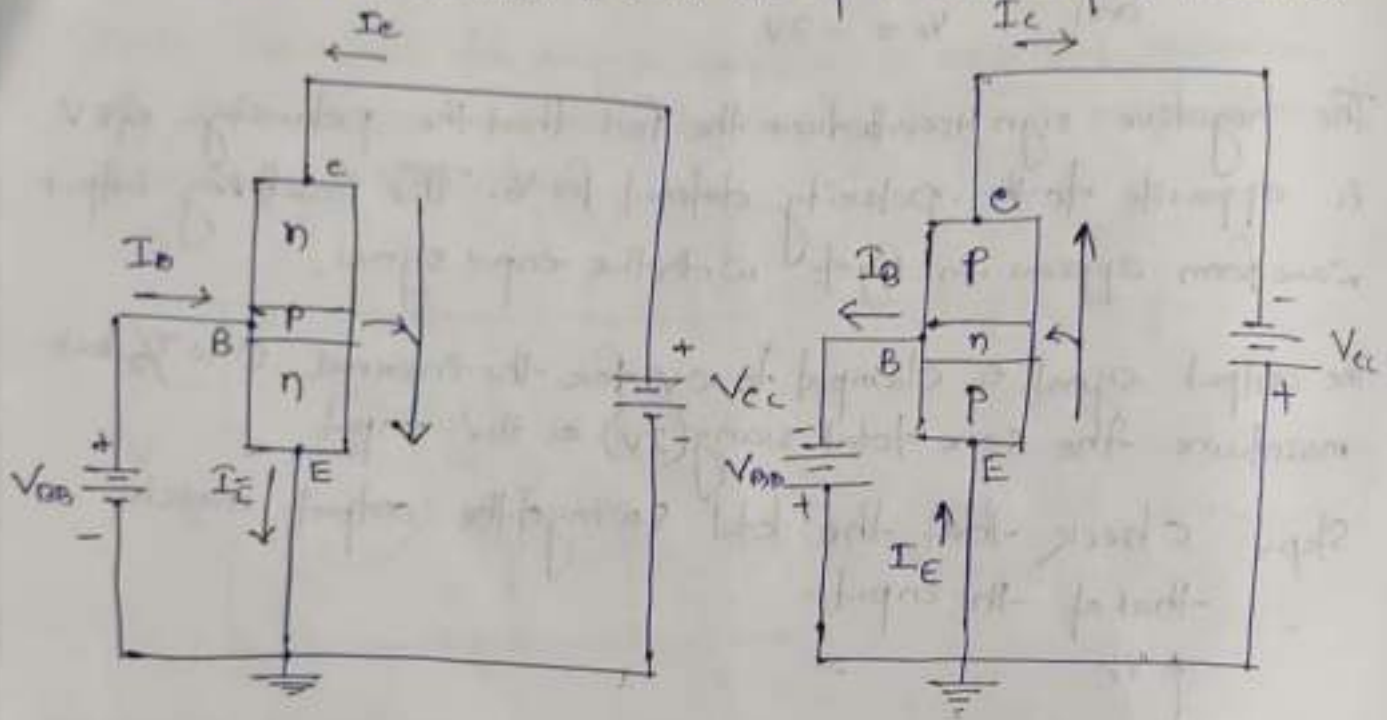
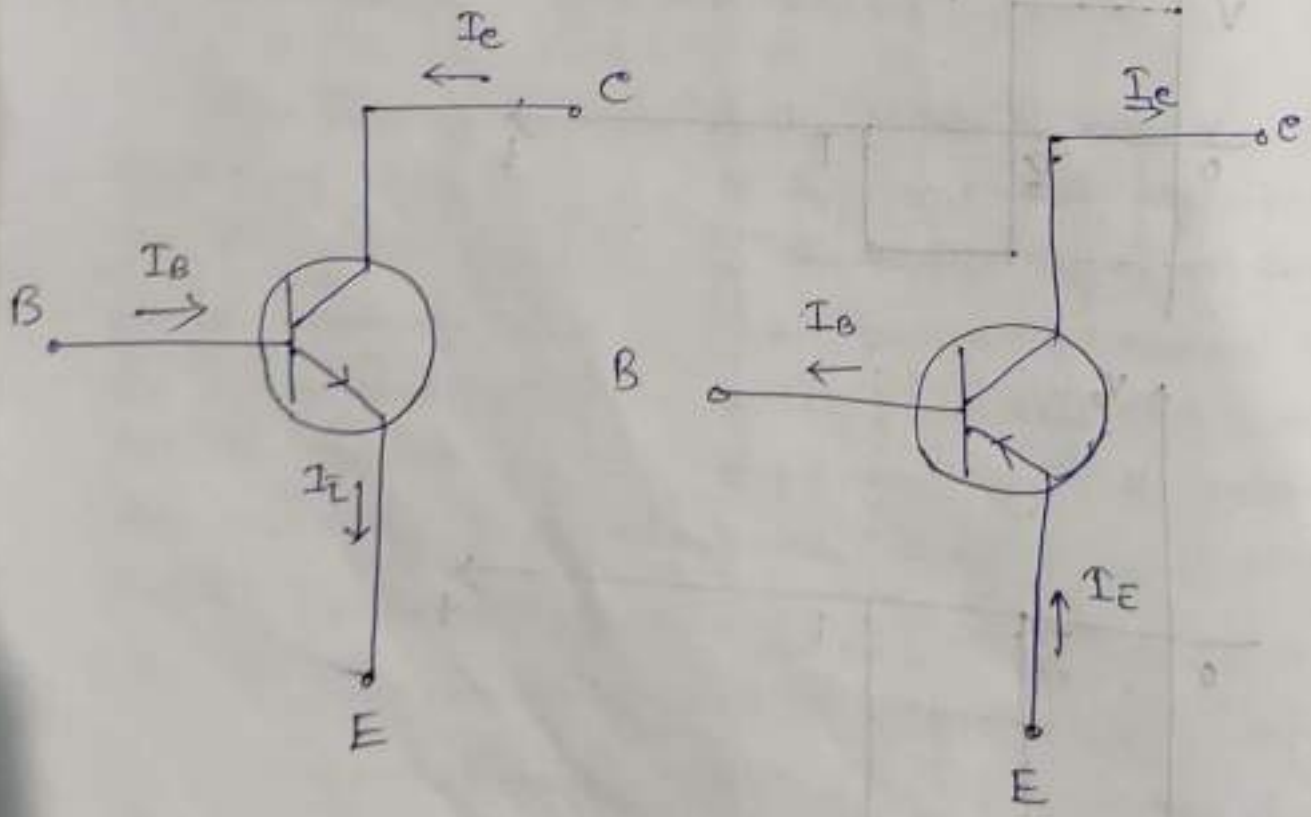
Common Emitter:

It is the most frequently encountered transistor configuration.

It is called the common-emitter configuration because the emitter is common to both the input and output terminals





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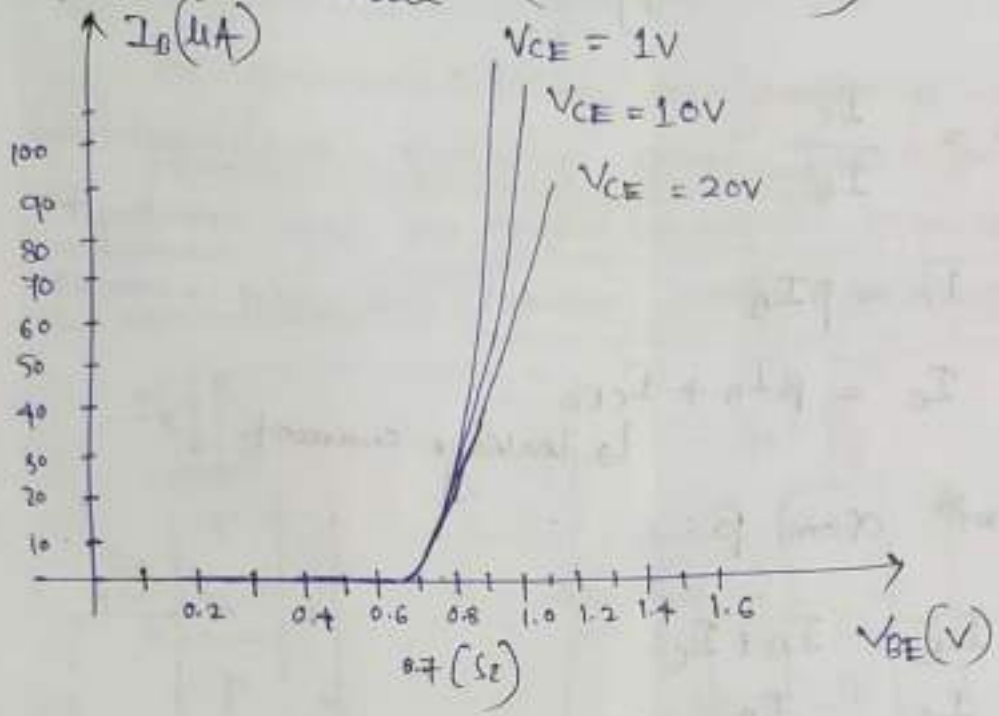
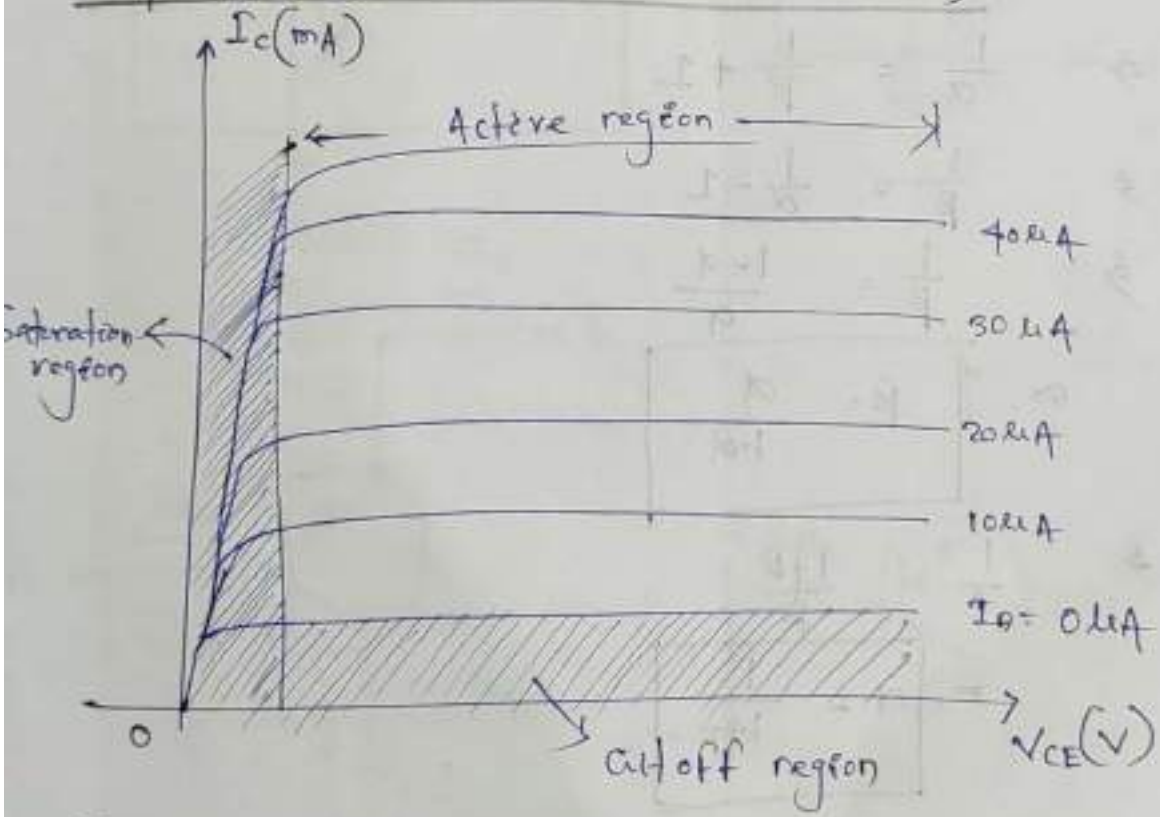
Input characteristics: (Common Emitter)



Output characteristics (Common Emitter):



In common Emitter, when input current I_B is zero then output current I_C is not equal to zero.

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Amplification factor or Current gain (for common Emitter)

$$\beta = \frac{I_C}{I_B}$$

$$\Rightarrow I_C = \beta I_B$$

$$\Rightarrow I_C = \beta I_B + I_{CEO}$$

↳ leakage current.

Relation btn α and β:

$$I_E = I_B + I_C$$

$$\Rightarrow \frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\Rightarrow \frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\Rightarrow \frac{1}{\beta} = \frac{1}{\alpha} - 1$$

$$\Rightarrow \frac{1}{\beta} = \frac{1-\alpha}{\alpha}$$

or, $\boxed{\beta = \frac{\alpha}{1-\alpha}}$

$$\Rightarrow \frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

or, $\boxed{\alpha = \frac{\beta}{1+\beta}}$

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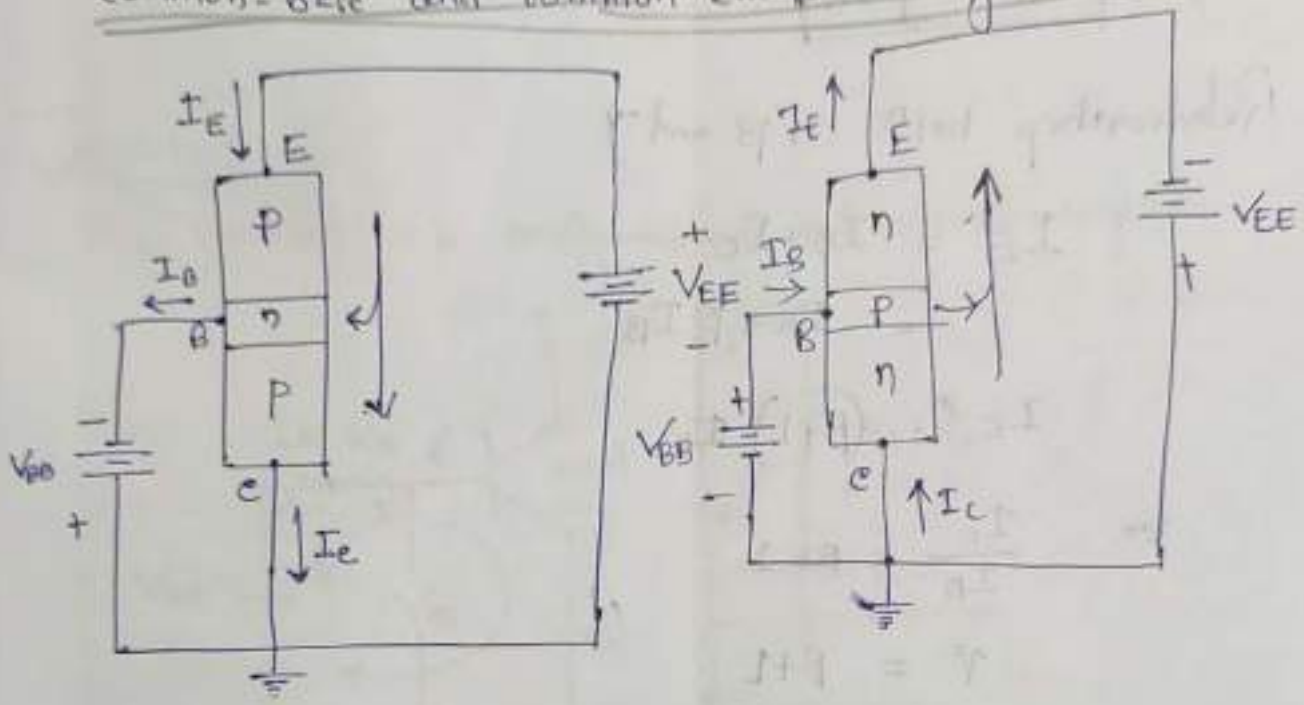
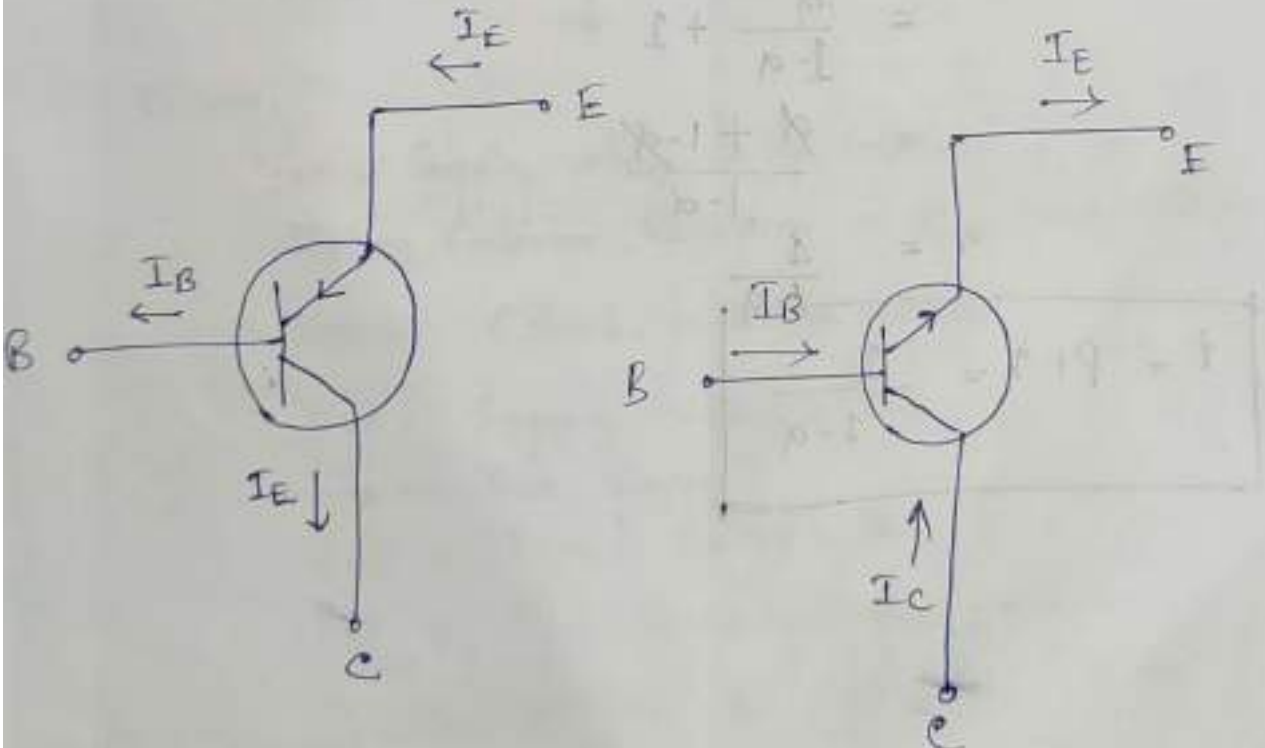
Common Collector Configuration:

The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common emitter configurations.





→ The characteristics of common Collector is same as common emitter

Common Collector Amplification factor or Current gain

$$\gamma = \frac{I_E}{I_B}$$

$$\Rightarrow \boxed{I_E = \gamma I_B} \qquad \gamma \gg 1$$

Relationship b/w α, β and γ

$$I_E = I_B + I_C$$

$$= I_B + \beta I_B$$

$$I_E = (\beta + 1) I_B$$

or, $$\frac{I_E}{I_B} = \beta + 1$$

$$\boxed{\gamma = \beta + 1}$$

$$= \frac{\alpha}{1-\alpha} + 1$$

$$= \frac{\alpha + 1 - \alpha}{1-\alpha}$$

$$\gamma = \frac{1}{1-\alpha}$$

$$\boxed{\gamma = \beta + 1 = \frac{1}{1-\alpha}}$$

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Date: 15/10/19

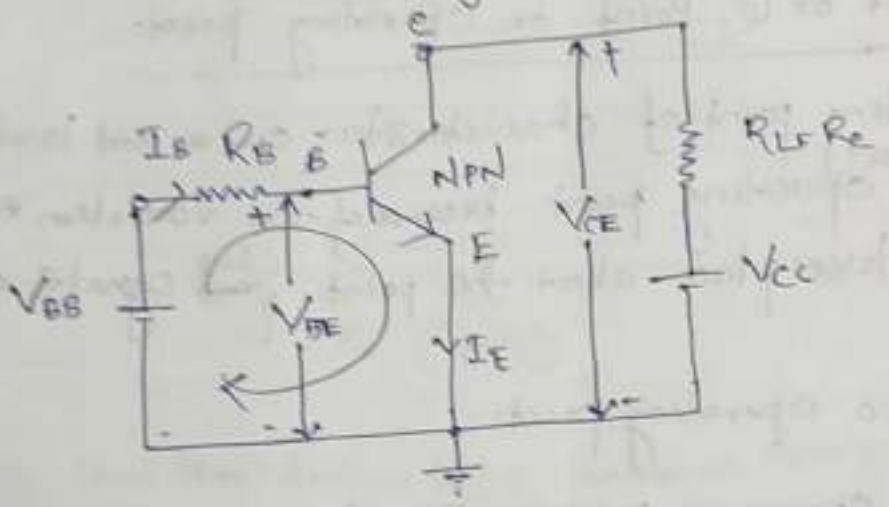
Transistor load line analysis:

DC load line analysis:

The method for finding out I_C (output current) values for different values of V_{CE} in absence of ac signal.

DC load line:

Consider CE ~~configuration~~ NPN transistor amplifier.



Where,

V_{cc} = Supply voltage to the Collector

R_c = Collector Resistance or R_L = load resistance

V_{CE} = Collector to Emitter voltage

V_{BB} = Supply voltage to Base

I_b = Base Current

V_{BE} = Base to Emitter voltage.

R_B = Base Resistance / Input resistance.

The DC load line gives the value of V_{CE} and I_C when AC signal is ~~on~~ off.

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AC load line:

When an a.c. signal is applied the transistor voltage V_{CE} and Collector current I_C varey above and below its the Quiescent Point Q or operating point. So point Q is common for both DC and AC load line.

The AC loadline gives the value of V_{CE} and I_C, when an a.c signal is applied.

Quiescent Point or Q-Point or Operating point:

Intersecting point of characteristics curve and load line. It is also called operating point because of the variation in V_{CE} and I_C takes place about this point when signal is applied

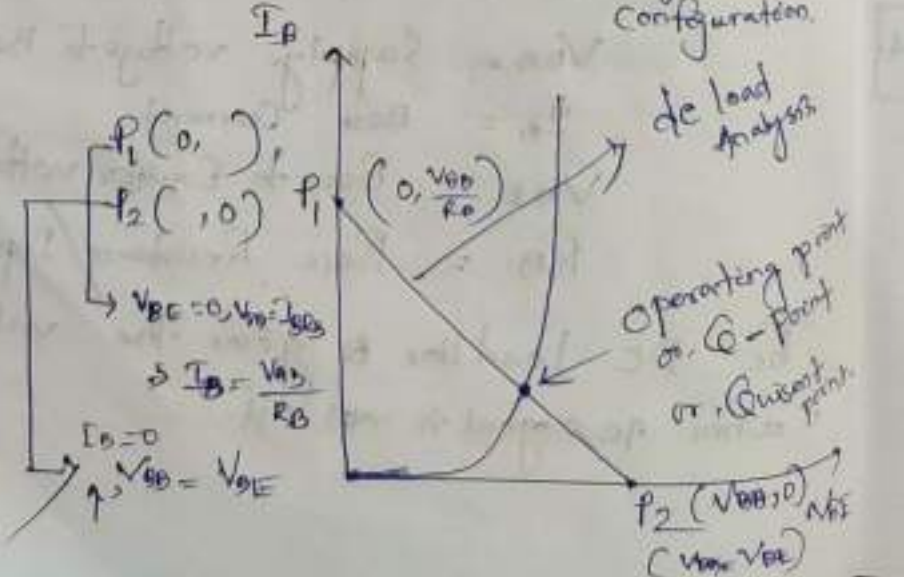
There are two operating point:

① output operating point.
apply KVL

② input operating point.
apply KVL,

$$-V_{BB} + I_B R_B + V_{BE} = 0$$

I/p characteristics of CE configuration.



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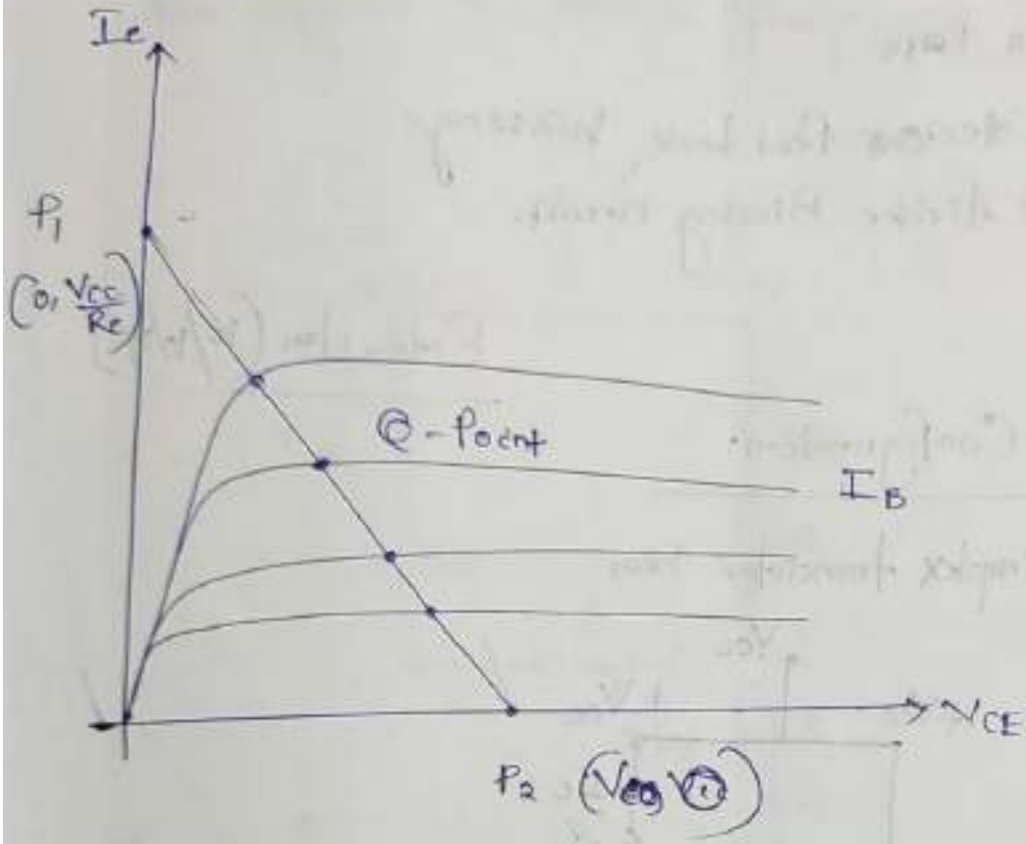
Output characteristics & operating point: (DC load line Analysis)

$V_{cc} - I_C R_C - V_{CE} = 0$



$P_1(0, ?)$, $V_{CE}=0$, $I_C = \frac{V_{cc}}{R_c}$

$P_2(?, 0)$, $I_C = 0$, $V_{cc} = V_{CE}$

$P_1\left(0, \frac{V_{cc}}{R_c}\right)$

$P_2(V_{cc}, 0)$

AC load line Analysis & DC loadline Analysis:

* AC load line is steeper than DC load line. But the two lines intersect at the Q-Point, determined by the biasing voltage and current.

* AC load line takes into the account the ac load resistance while the DC load line consider only DC resistance.

Transistor Biasing:

Def. External DC voltage applied to the transistor. ie. is called Transistor Biasing.

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There are four type of Biasing in BJT - Transistor.

1. fixed Bias
3. Emitter Base
3. DC Collector feed back biasing
4. Voltage divider Biasing circuit.

Extra class (1c/b/19)

① fixed - Bias Configuration:

* It is the simplex transistor bias

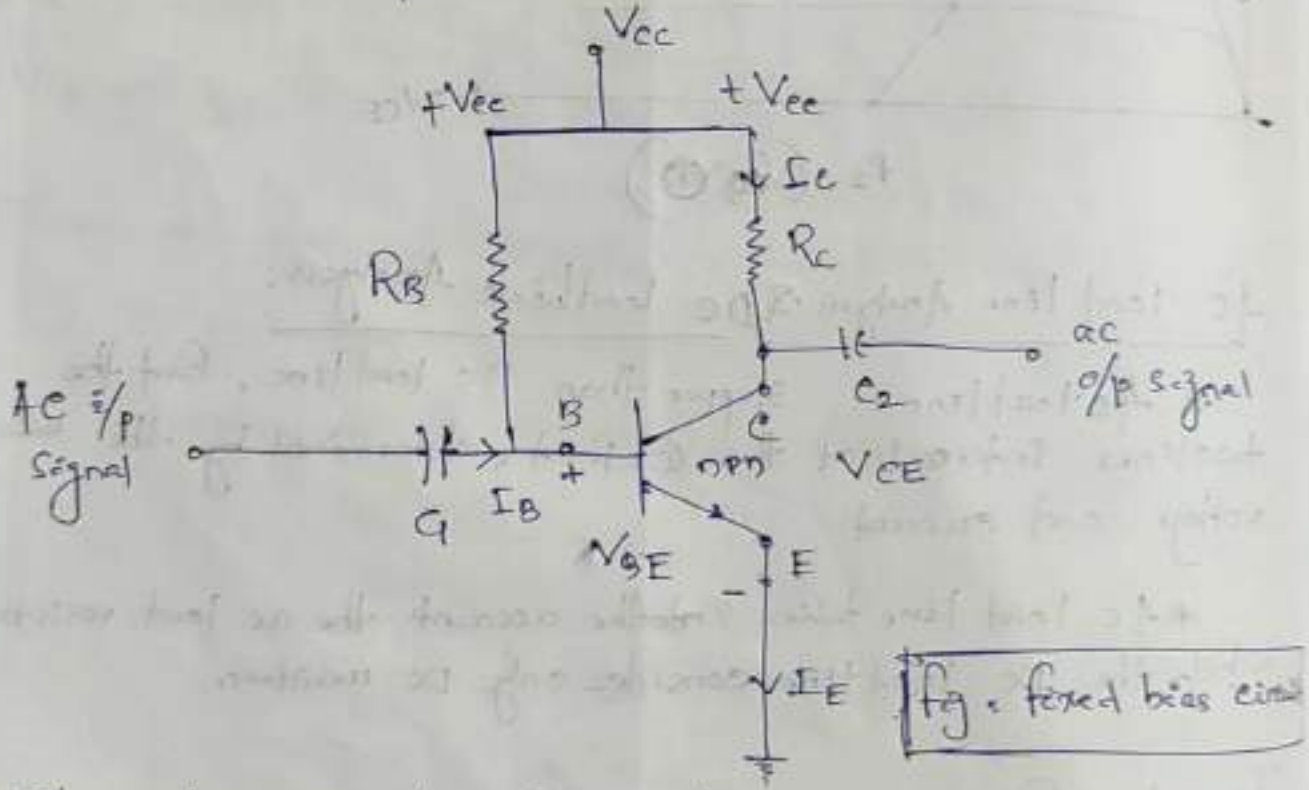

fig. fixed bias circ

* It is also known as base biase Network
* For the dc analysis ac input removed and as well as capacitor

f = 0-Hz · Capacitive reactance

$X_C = \frac{1}{2\pi fc}$

$= \frac{2}{2\pi(0)c} = \infty$

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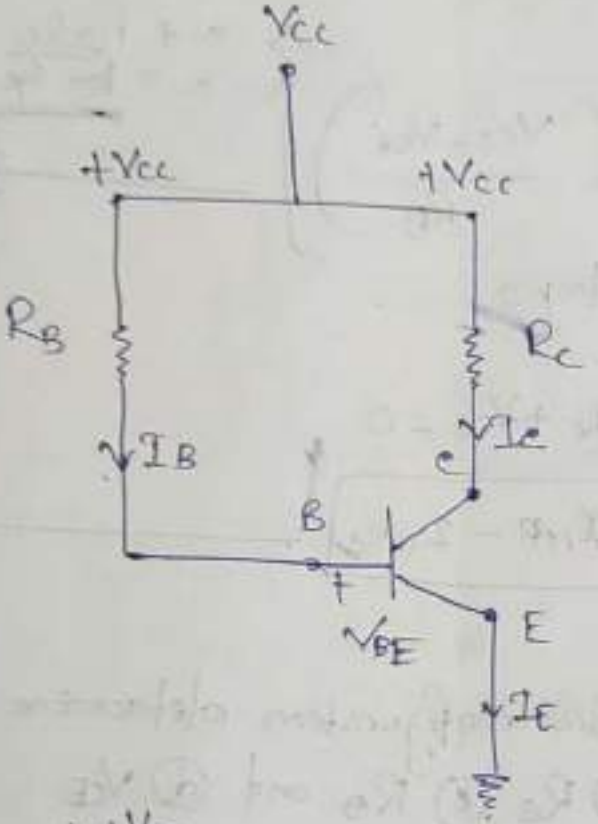
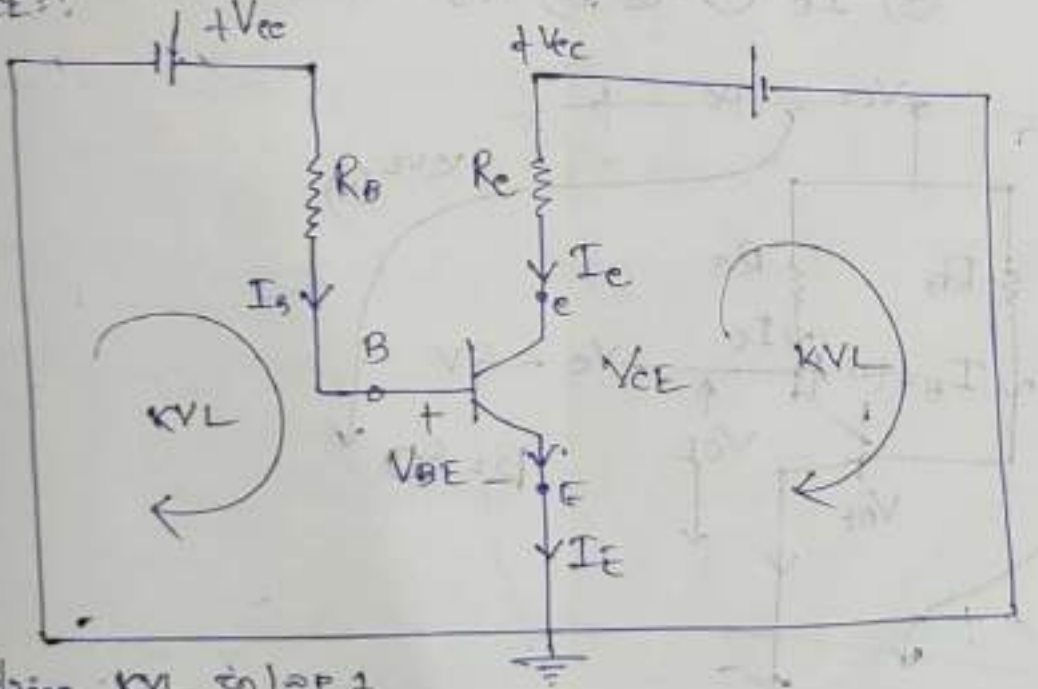
for DC Analysis:

In addition, the dc supply V_{cc} can be separated into two supplies (for analysis purpose only)



$I_C = ?$

$V_{CE} = ?$



Applying KVL in loop 1.

$$-V_{cc} + I_B R_B + V_{BE} = 0$$

$$I_B = \frac{1}{\beta} I_c$$

$$I_c = \beta I_B$$

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$$I_B R_B = V_{CC} - V_{BE}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$$

$$\boxed{I_C = \beta I_B}$$

0.7 for Si
0.3 for Ge

or, $\boxed{I_C = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right)}$ ——— (2)

Applying KVL to loop 2.

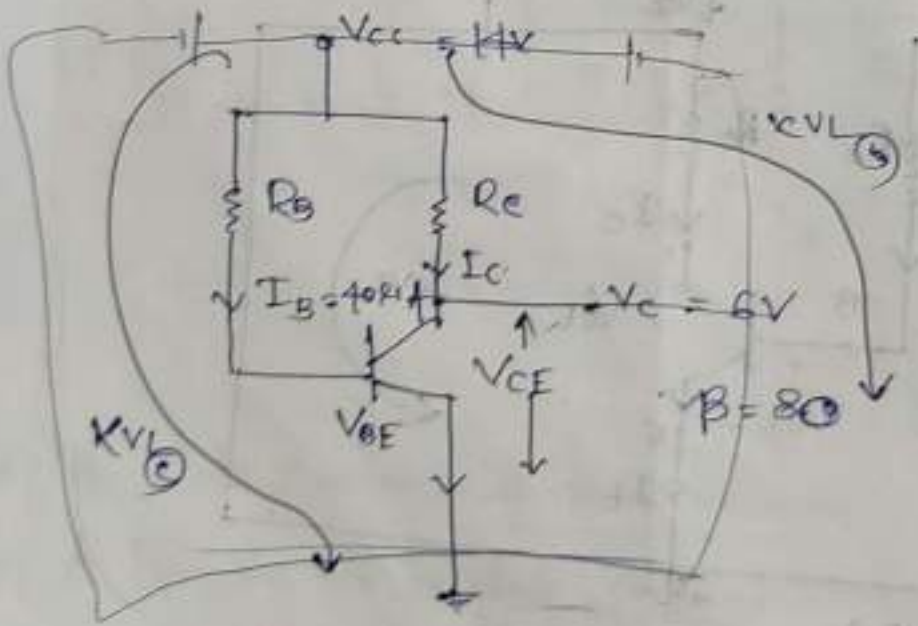
$$-V_{CE} - I_C R_C + V_{CC} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \quad \text{——— (3)}$$

Problem: (1)

For the fixed Bias configuration determine

(a) I_C (b) R_C (c) R_B and (d) V_{CE}



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Given data,

$V_{cc} = 14V$

$I_B = 40\mu A$

$\beta = 80$

$V_c = 6V$

(a) $I_c = \beta I_B$ ~~V_{ee}~~

$I_c = \beta I_B$

$= 80 \times 40 \times 10^{-6} A$

$= 3200 \times 10^{-6} A$

$= 0.0032 A$

$= 3.2 \times 10^{-3} A$

$\therefore I_c = 3.2 \times 10^{-3} A$

or, $I_c = 3.2 mA$ (Ans)

(b) Applying KVL

$V_{ee} - I_c R_c - V_c = 0$

$14V - (3.2 \times 10^{-3}) R_c - 6V = 0$

$3.2 \times 10^{-3} R_c = 8V$

$R_c = 2500 \Omega$,

or, $R_c = 2.5 K\Omega$ (Ans)

(c) $R_B = ?$

Applying KVL,

here $V_{BE} = 0.7$

$V_{cc} - I_B R_B - V_{BE} = 0$

$R_B = \frac{V_{cc} - V_{BE}}{I_B} = \frac{14 - 0.7}{40\mu A} = 332500 \Omega$

$= 332.5 K\Omega$

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(d) $V_{CE} = ?$

$$-V_{CE} - I_C R_C + V_{CC}$$

$$V_{CC} - I_C R_C = V_{CE}$$

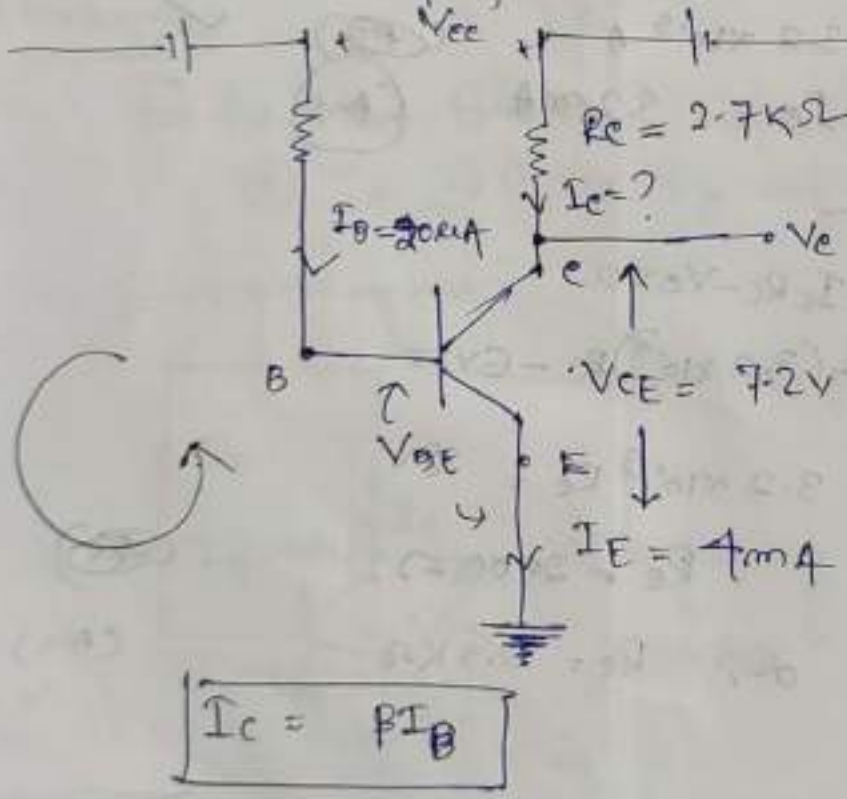
$$14 - \left((3.2 \times 10^{-3} A) \times 2.5 \times 10^{3} \Omega\right) = V_{CE}$$

$$V_{CE} = 6V \quad \text{(A)}$$

Problem (3): for the fixed bias configuration Determine.

(a) I_C (b) V_{CC} (c) β (d) R_B

$I_B = 20\,\mu A$, $R_C = 2.7\,K\Omega$, $V_{CE} = 7.2V$, $I_E = 4mA$



$$I_C = \beta I_B$$

$$\beta = \frac{I_C}{I_E}$$

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$V_{cc} - V_{BE} - I_B R_B = 0$

$V_{cc} - V_{BB} - (20\,\mu A \times R_B) = 0$

$V_{cc} - I_c R_c$.

(a) $I_c = ?$

$I_E = I_B + I_c$

$I_c = I_E - I_B$

$= 4\,mA - 20\,\mu A$

$= 4\,mA - 0.02\,mA$

$= 3.98\,mA$ Ans

(a) $I_c \simeq I_E + I_B$

$= 4\,mA + 20\,\mu A$

$= 4 \times 10^{-3} + 20 \times 10^{-6}$

$= 4.02 \times 10^{-3}\,A$ or $4.02\,mA$

Note: $I_c \simeq I_E$

(b) $V_{cc} - V_{CE} - I_c R_c = 0$

$V_{cc} = V_{CE} + I_c R_c$

$= 7.2\,V + (3.98\,mA \times 2.7\,k\Omega)$

$= 7.2\,V + 10.746\,V = 17.946\,V$

$\therefore V_{cc} = 17.946$ (m)

(c) $\beta = \frac{I_c}{I_B}$ for Common Emitter

$= \frac{3.98\,mA}{20\,\mu A} = 0.199 \times 10^3 = 199$

$\therefore \beta = 199$

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(1) $V_{CC} - V_{BE} - I_B R_B = 0$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

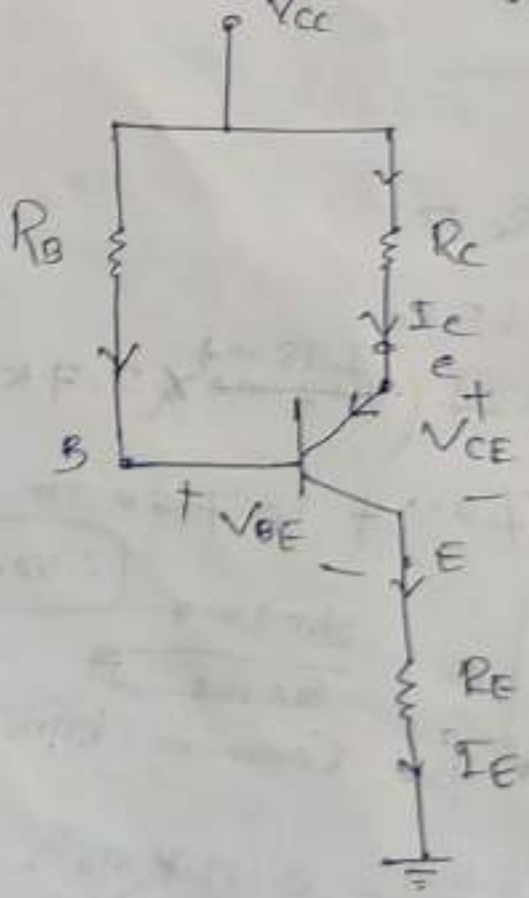
$$= \frac{17946 - 0.7}{20\mu A}$$

$$= 862300\,\Omega$$

$$\therefore R_B = 862.3\,k\Omega$$

(3) Emitter Base Configuration:

The dc bias network contains an Emitter resistor to improve the stability level of operating point over the fixed bias configuration.



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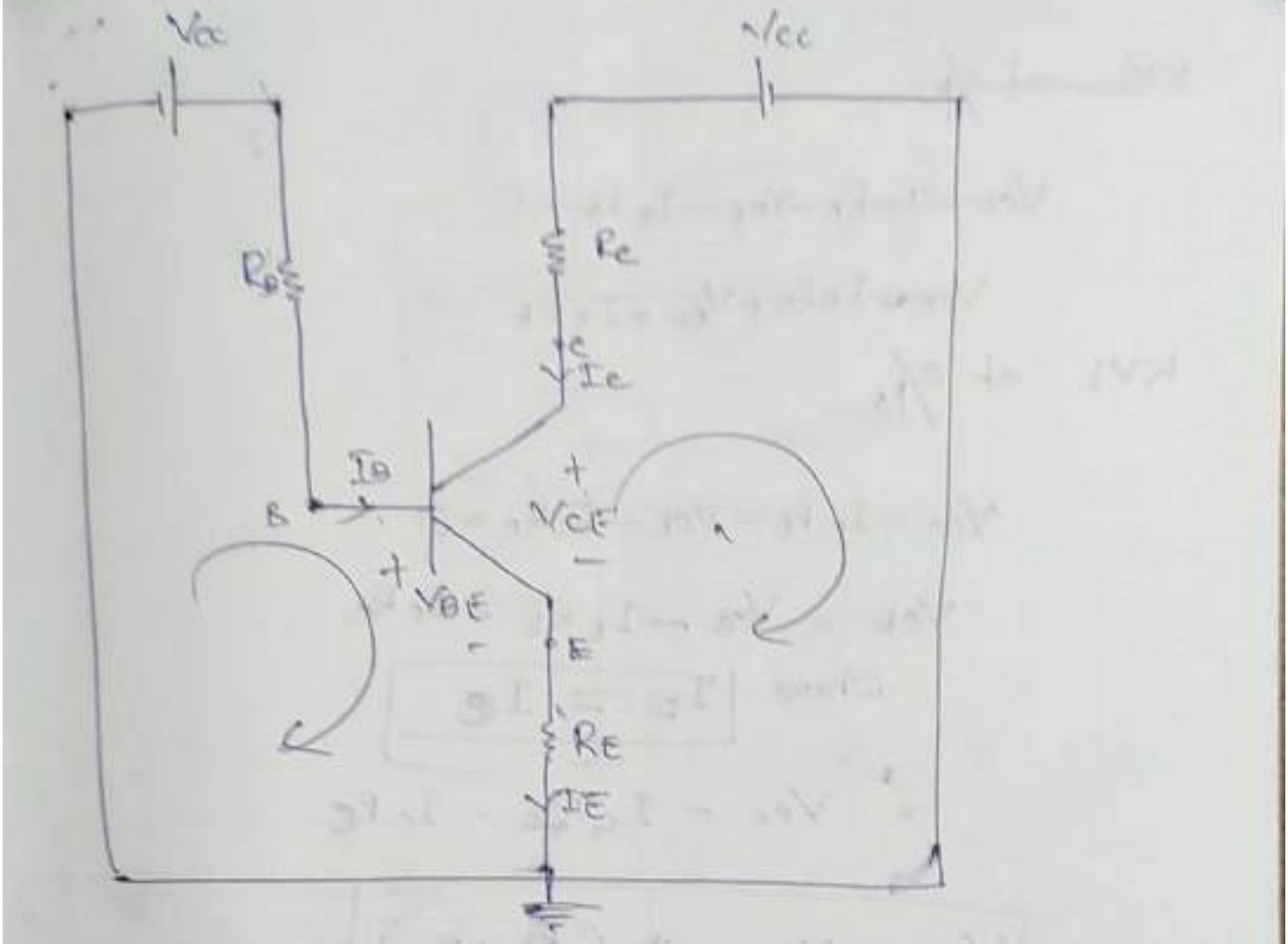

KVL at i/p.

$$-V_{cc} + I_B R_B + V_{BE} + I_E R_E = 0$$

$$I_E = I_C + I_B$$

$$I_C = \beta I_B$$

$$\therefore I_E = \beta I_B + I_B$$

$$I_E = (\beta + 1) I_B$$

$$-V_{cc} + I_B R_B + V_{BE} + (\beta + 1) I_B R_E = 0$$

$$-V_{cc} + I_B (R_B + (\beta + 1) R_E) + V_{BE} = 0$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$\text{or, } I_C = \beta \left(\frac{V_{cc} - V_{BE}}{R_B + (\beta + 1) R_E} \right)$$

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~~KVL at o/p:~~

~~$V_{cc} - I_B R_B - V_{BE} - I_E R_E = 0$~~

~~$V_{cc} = I_B R_B + V_{BE} + I_E R_E$~~

KVL at o/p:

$$V_{cc} - I_E R_E - V_{CE} - I_c R_c = 0$$

$$V_{CE} = V_{cc} - I_E R_E - I_c R_c$$

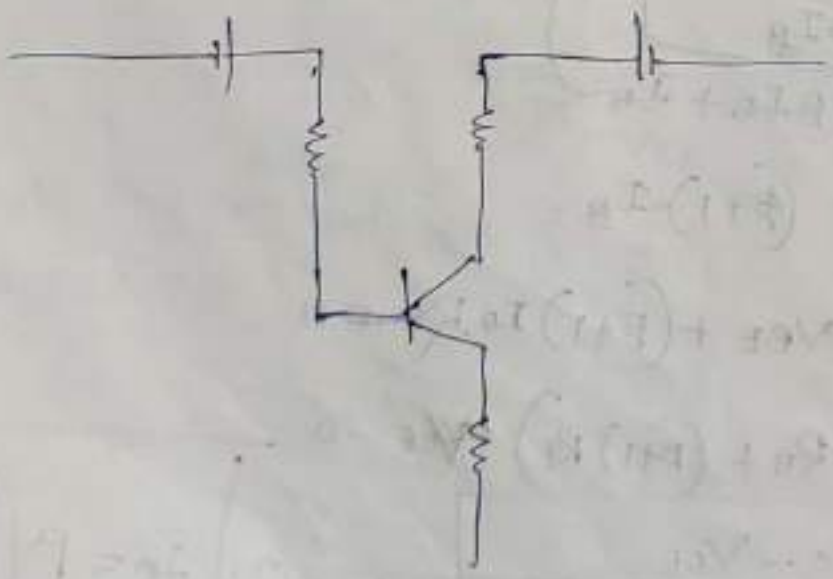
where $\boxed{I_E \simeq I_c}$

$$= V_{cc} - I_c R_E - I_c R_c$$

$$\boxed{V_{CE} = V_{cc} - I_c (R_E + R_c)}$$

Problem: (3) In the Emitter Bias network, Determine

(a) I_B (b) I_c (c) V_{CE} (d) V_c (e) V_E (f) V_B (g) V_{BE}



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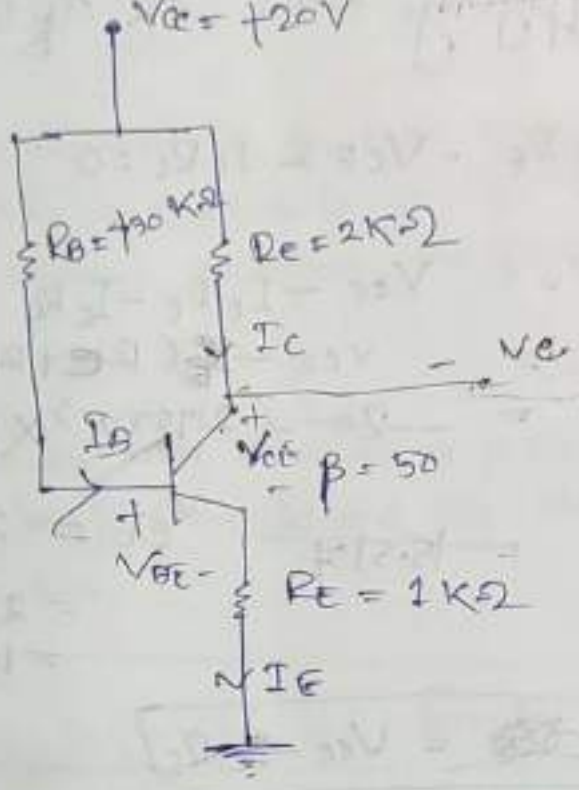
Vc.



(a) $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E}$

$= \dfrac{20 - V_{BE}}{430\times10^3 + (50+1)\,1K\Omega}$

$= \dfrac{20 - V_{BE}}{430\times10^3 + 51}$ (there, $V_{BE} = 0.7$)

$= \dfrac{20 - 0.7}{430\times10^3 + 51K\Omega} = \dfrac{19.3}{481K\Omega} = 40.12\mu A$

(b) $I_C = \beta I_B = 50 \times I_B = 2.248\times10^{-3}\,A$

$I_E = I_C - I_B$

$= 2.19813\times10^{-3}\,A$

$\Rightarrow I_C = \beta I_B$

$= 50(40.12\mu A)$

$= 2\,mA$

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(2) V_{CE} =? - Applying KVL at o/p side.

$V_{cc} - I_E R_E - V_{CE} - I_C R_C = 0$ $\quad (\because I_C \simeq I_E)$

$V_{CE} = V_{cc} - I_E R_E - I_C R_C$

$= V_{cc} - I_E(R_E + R_C)$

$= 20 - (2.179 \times 10^{-3} \times 1) - (2.249 \times 10^{-3} \times 2 \times 10^3)$

$= 15.517$

$V_{CE} = 20 - (2.01\,mA)(2k\Omega)$

$= 20V - 6.03V$

$= 13.97V$ ——— (b)

(4) $V_C = V_{cc} - I_C R_C$

$V_e = V_{cc} - I_E R_C = 20 - (2.01\,mA)(2k\Omega)$

$= 20 - 4.02V$

$= 15.98V$ ——— (a)

$= 20 - (2.249 \times 10^{-3} \times 2 \times 10^3)$

(5) $V_E = V_e - V_{cc} = 15.517$

$= 15.98V - 13.97V = 2.01V$ ——— Ans

(6) $V_{BE} = V_B - V_E$

$\Rightarrow V_B = V_{BE} + V_E$

(7) $V_B = V_{BE} + V_E = 0.7V + 2.01V$

(8) $V_{BC} = V_B - V_C = 2.71V$ ——— Ans

$= 2.71V - 15.98V$

$= -13.27V$ ——— Ans

$-V_{cc} + I_B R_B + V_{BE} + I_E R_E = 0$

$\Rightarrow V_{cc} = I_B R_B + V_{BE} + I_E R_E$

$\Rightarrow V_{BE} = V_{cc} - (I_B R_B + I_E R_E)$

$= 20 - (4.18 \times 10^{-5} \times$

In a fix
whenever
and thus
Saturation
$\rightarrow$ In ca
maintain
again B

Fixed
Constant
I_B
$\beta\uparrow$, I

(3) Collector feed

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Stability

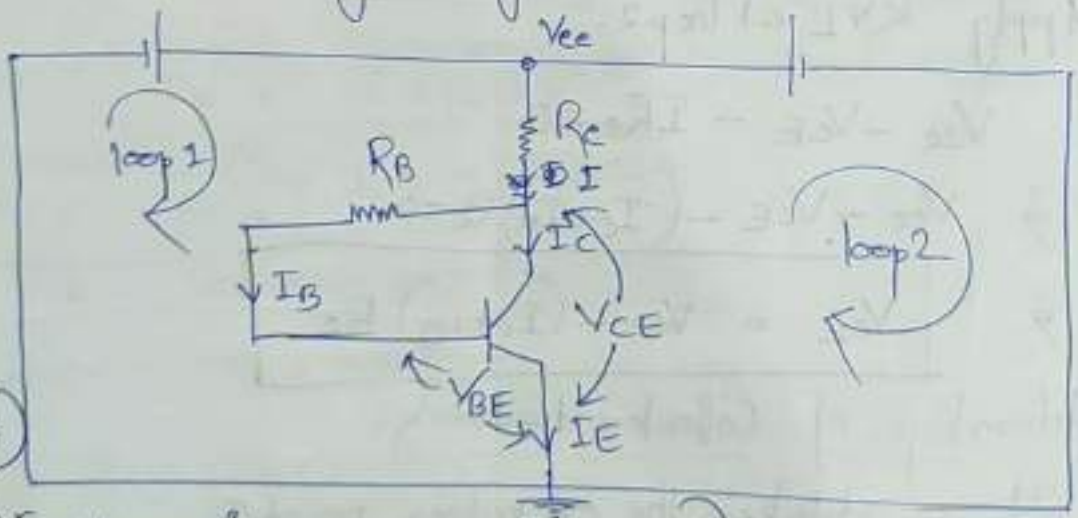
Date: 17/10/19

In a fixed bias current I_B does not vary with β and therefore whenever there is an increase in β, I_C increases proportionally and thus V_{CE} reduces making the Q-point to drift towards saturation.

In an emmitter bias current as β increases I_B reduces maintaining almost same I_C and V_{CE} stabilising the Q-point again β-variation.

Fixed bias	Emitter bias
Constant I_B does not vary with β $\beta\uparrow, I_C\uparrow \rightarrow V_{CE}\downarrow$	$\beta\uparrow, I_B\downarrow$, I_C and V_{CE} constant

(3) Collector feedback biasing Configuration:



$I_B R_B + I_E R_E$

$4.78 \times 10^{-5} \times 490 \times 10^3 + 2.178 \times 10^{-5} \times 1 \times 10^3$

An improved level of stability can also be obtained by introducing a feedback path from Collector to base as shown in fig.

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→ Sensitivity of Q-point to changes in β temperature variation is normally less than that encountered, for the fixed bias and or emitter bias configuration.

KVL at loop 1:

$$-V_{cc} + IR_e + I_B R_B + V_{BE} = 0$$

$$\Rightarrow -V_{cc} + (I_B + I_c) R_e + I_B R_B + V_{BE} = 0$$

$$I_e = \beta I_B$$

$$\Rightarrow -V_{cc} + (I_B + \beta I_B) R_e + I_B R_B + V_{BE} = 0$$

$$\Rightarrow -V_{cc} + I_B (1+\beta) R_e + I_B R_B + V_{BE} = 0$$

$$\Rightarrow -V_{cc} + I_B [(1+\beta) R_e + R_B] + V_{BE} = 0$$

$$\Rightarrow \boxed{I_B = \frac{V_{cc} - V_{BE}}{[(1+\beta) R_e + R_B]}}$$

Apply KVL at loop 2:

$$V_{cc} - V_{CE} - I R_e = 0$$

$$\Rightarrow V_{cc} - V_{CE} - (I_c + I_B) R_e = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{cc} - (I_c + I_B) R_e}$$

Advantages of Collector feedback:

It is stabilizes the operating point Q.

(i) against variation of temperature
(ii) against variation of biasing voltage
(iii) against variation of β

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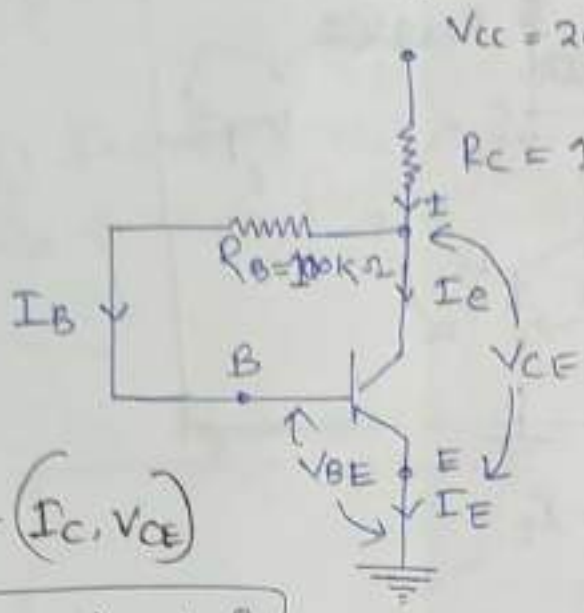
Problem: Fig shows Si transistore bias by Collector feedback method determine operating point or Q-point.



Q-Point = (I_C, V_{CE})

$$V_{BE} = V_B - V_E = 0.7V$$

$$\therefore V_B = 0.7V$$

We know $I_e = \beta I_B$

Applying KVL at B-E side

$$I_B = \frac{V_{CC} - V_{BE}}{(1+\beta)R_C + R_B} = \frac{20 - 0.7}{(1+100)\times 1\times 10^3 + 100\times 10^3}$$

$$= 0.0960\ mA$$

or, $I_B = 0.096\ mA$

or, $I_B = 96\ \mu A$.

$$I_e = \beta I_B$$

$$= 100 \times 0.096 \times 10^{-3}$$

$$I_e = 9.6\ mA$$

Applying KVL at O/P side

$$V_{CE} = V_{CC} - (I_C + I_B)R_C$$

$$= 20 - (9.6\times 10^{-3} + 0.096\times 10^{-3}) \times 1\times 10^3$$

$$= 10.304\ V$$

Operating point or, Q-Point = $(9.6mA, 10.304V)$

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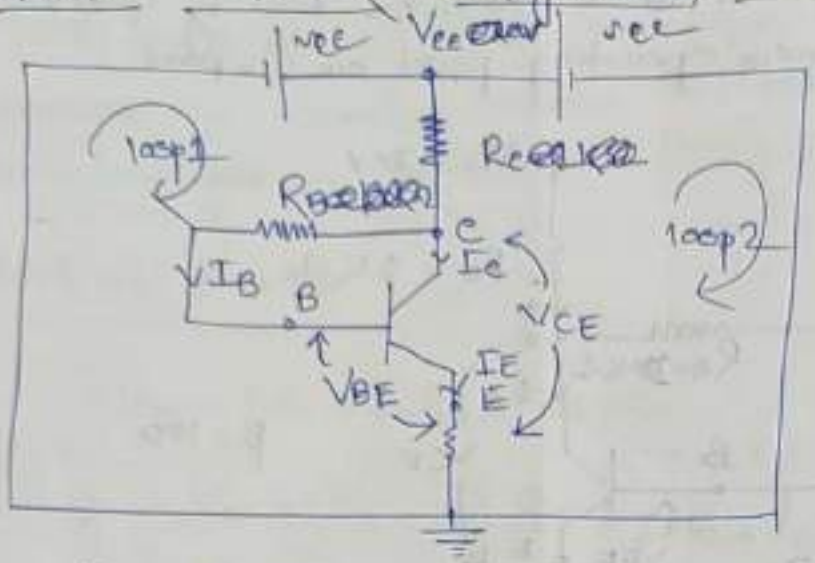
Collector Feedback configuration with Emitter Resistor



$I = I_C + I_B = I_E$

$I_E = I_C + I_B$

$= \beta I_B + I_B$

$= I_B(\beta + 1)$

Loop 1 Input loop:

$-V_{CC} + (I_B + \beta I_B) R_C + I_B R_B + V_{BE} + I_B(\beta+1) R_E = 0$

$\Rightarrow -V_{CC} + I_B(1+\beta) R_C + I_B R_B + V_{BE} + I_B(\beta+1) R_E = 0$

$\Rightarrow -V_{CC} + I_B[(\beta+1)(R_C + R_E) + R_B] + V_{BE} = 0$

$\Rightarrow$

$$I_B = \frac{V_{CC} - V_{BE}}{[(\beta+1)(R_C + R_E) + R_B]}$$

KVL at op loop:

$+V_{CC} - V_{CE} - I_{RC} - I_E R_E = 0$

$+V_{CC} - V_{CE} - I_E R_C - I_E R_E = 0$

$\Rightarrow V_{CC} - V_{CE} - I_E(R_C + R_E) = 0$

$\Rightarrow$

$$V_{CE} = V_{CC} - I_E(R_C + R_E)$$

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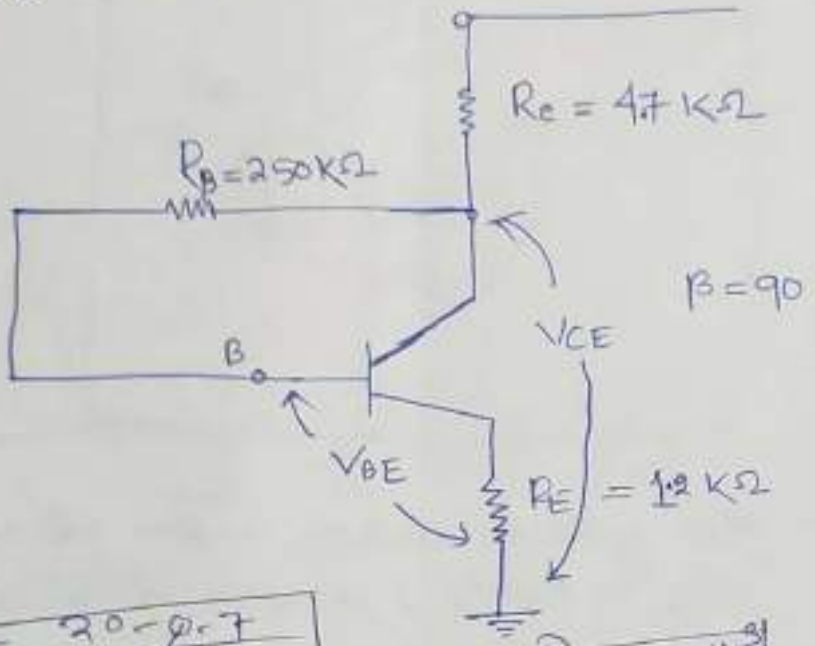
eq: $I_C = \beta I_B$

$$\therefore I_C = \beta \left(\frac{V_{CC} - V_{BE}}{(\beta+1)(R_C + R_E) + R_B} \right)$$

Problem (2) Determine the operating point in quiescent level I_{CQ} & V_{CEQ} for the network. $V_{CC} = 10V$



$$I_B = \frac{20 - 0.7}{(90+1)(4.7\times10^{3} + 1.2\times10^{3}) + 250\times10^{3}}$$

$$= \frac{19.03}{90(5.9\times10^{3}) + 250\times10^{3}}$$

$$= 3.4547 \times 10^{-3} \times 10^{-1}$$

$$I_C = \beta I_B = 90 \times 6.098\times10^{-4}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{10 - 0.7}{250K\Omega + 90(4.7+1.2)K\Omega}$$

$$= \frac{9.3}{781K\Omega} = 11.9\mu A$$

$$I_C = \beta I_B = 90(11.90)\mu A = 1.07mA$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 10 - 1.07mA(4.7K\Omega + 1.2K\Omega)$$

$$= 10 - 6.31 = 3.69V$$

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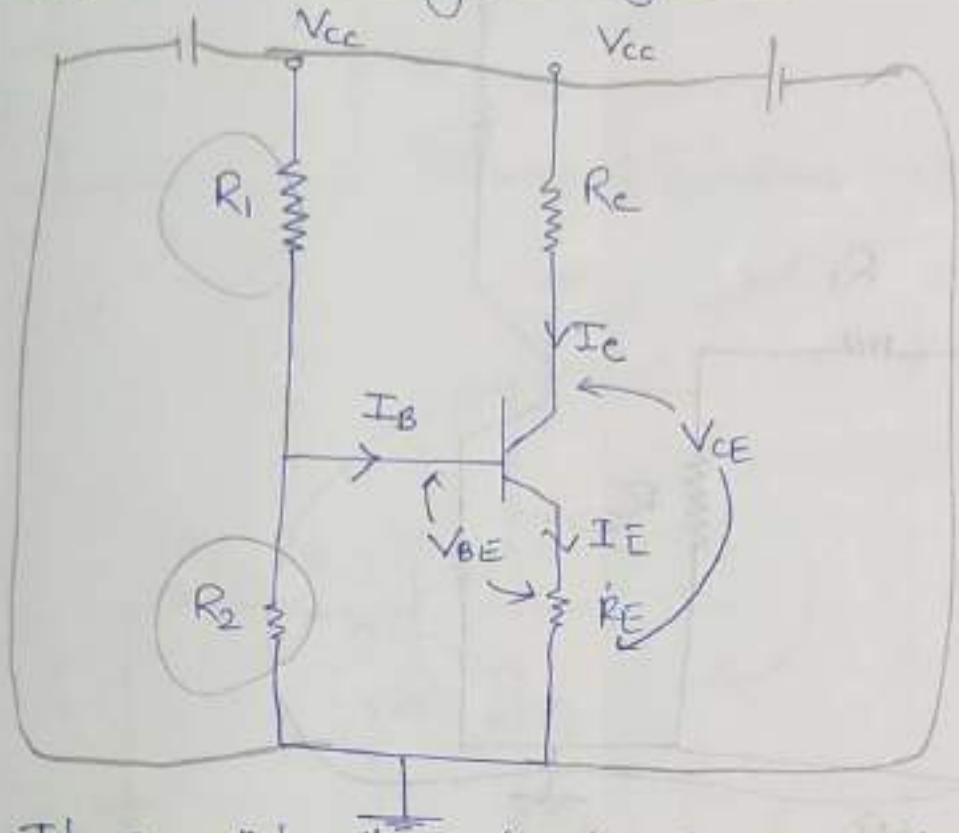
Voltage devider biasing configuration:



★ It is called voltage devider biasing network, because of voltage devider network (shown in R_1 & R_2) is used to transistor bias.

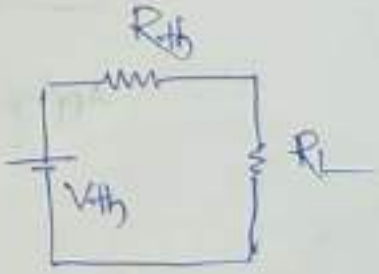
★ It is most widely used bias

★ This is biasing ckt. where I_{CQ} and V_{CEQ} (ie operating point) are almost independent of β.

★ The level of I_{BQ} will change with β so as to maintain the value of I_{CQ} and V_{CEQ} almost same so that stability is good for I_C and V_{CE}?

Two methods

① Exact methods ⇒ Thevenin's Theorem



③ Approximate method

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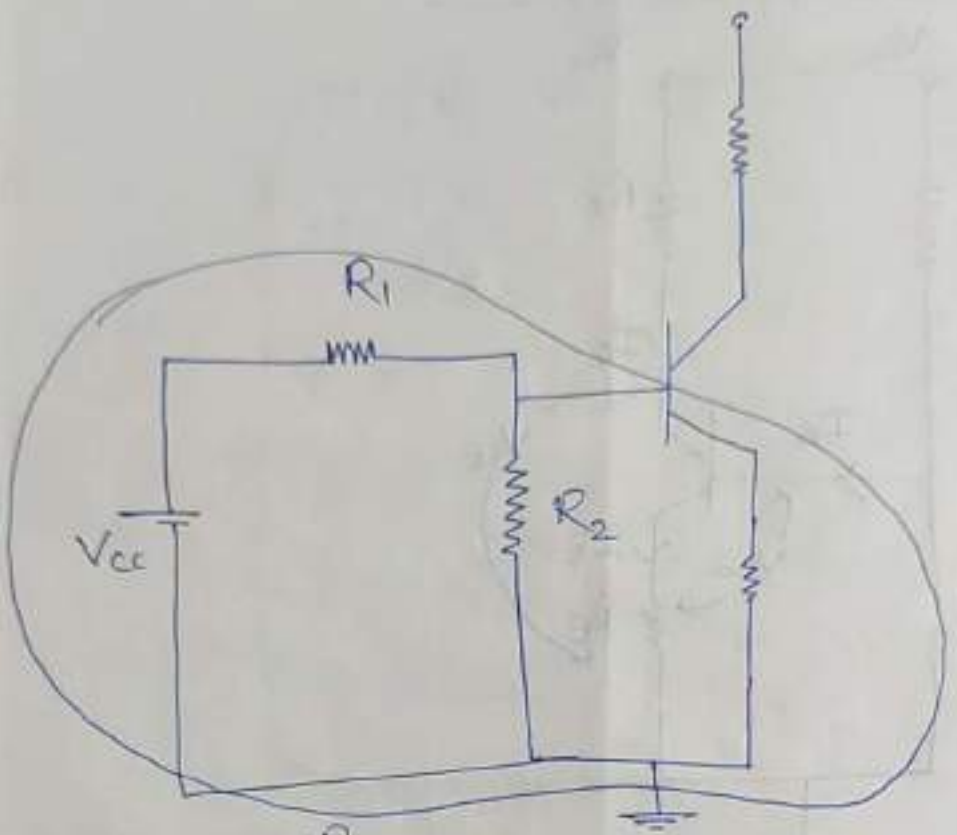

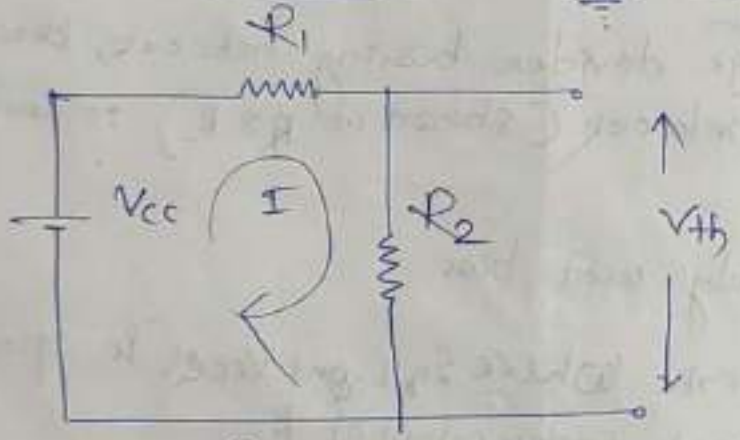

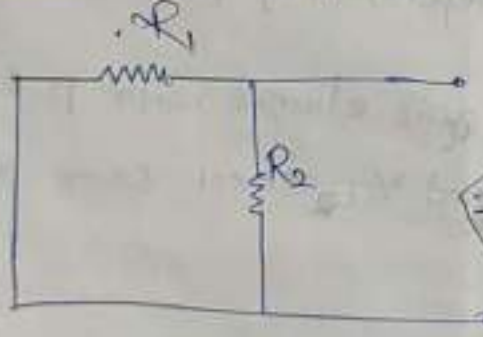

$$\therefore R_{th} = \frac{R R_2}{R_1 + R_2}$$

Apply KVL, $-V_{cc} + I R_1 + I R_2 = 0$

$$I = \frac{V_{cc}}{R_1 + R_2}$$

So, $$V_{th} = I R_2 = \frac{V_{cc} R_2}{R_1 + R_2}$$

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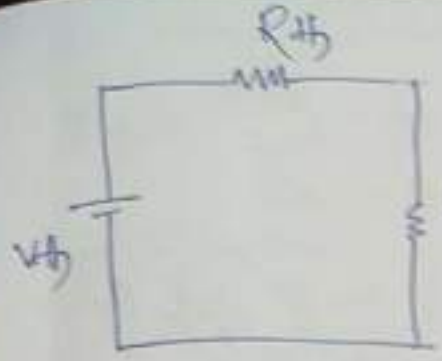
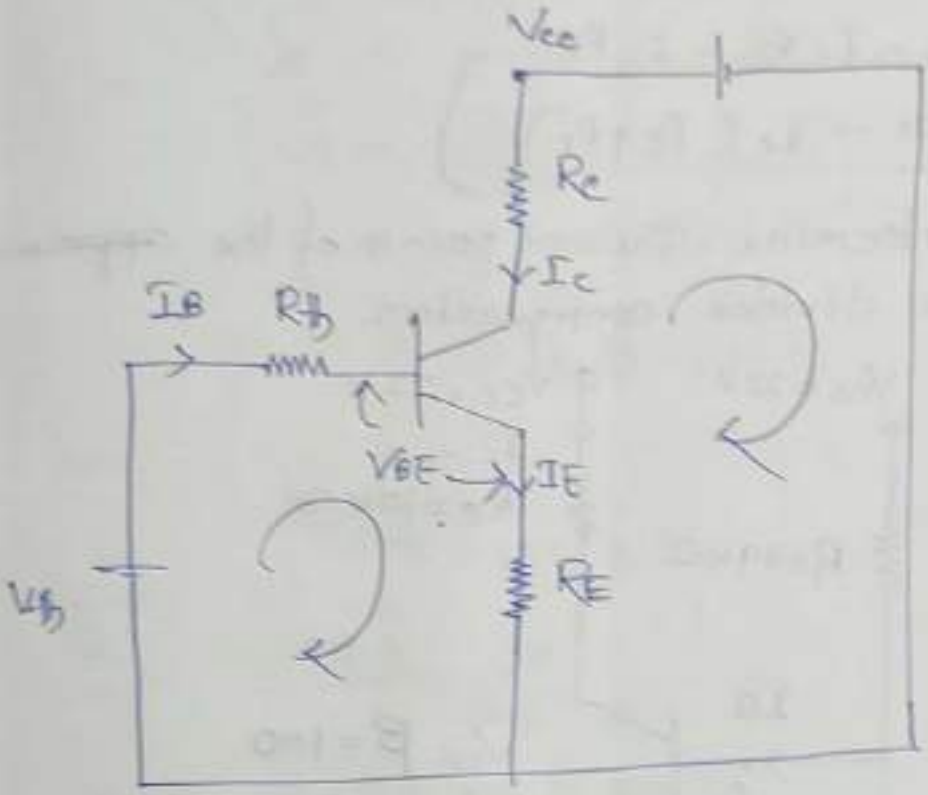


Thevenin Equivalent ckt.



KVL at i/p loop.

$$-V_{th} + I_B R_{th} + V_{BE} + I_E R_E = 0$$

$$I_E = (1+\beta) I_B$$

$$-V_{th} + I_B R_{th} + V_{BE} + (1+\beta) I_B R_E = 0$$

$$-V_{th} + I_B \left[R_{th} + (1+\beta) R_E \right] + V_{BE} = 0$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1+\beta) R_E}$$

$$I_c = \beta I_B$$

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KVL at o/p loop.

$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0$

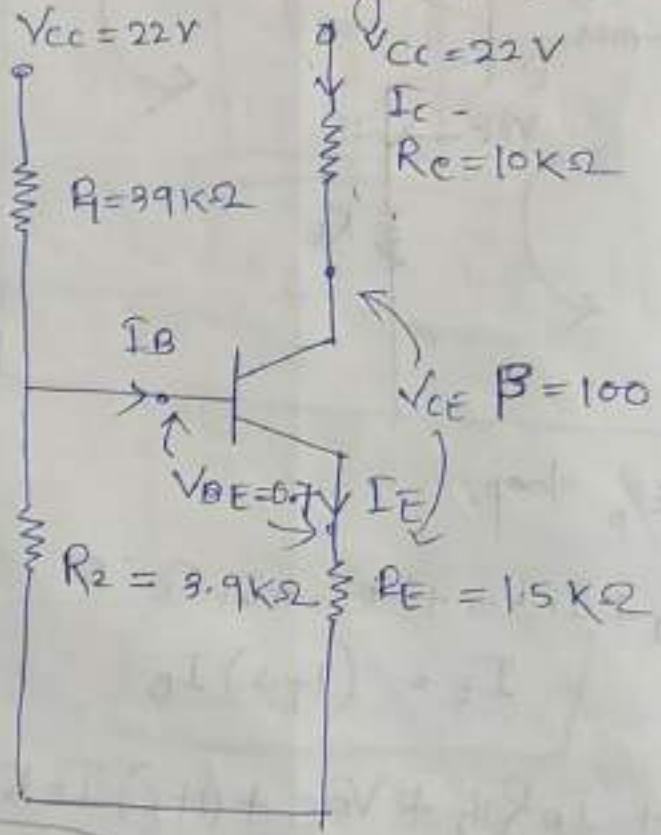
$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$V_{CE} = V_{CC} - I_C R_C - I_C R_E$

$V_{CE} = V_{CC} - I_C (R_C + R_E)$

$I_C = I_E$

Problem: Determine Quisent points of the ~~mod~~ voltage devider configurateon.



$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{(39 \times 3.9)\,K\Omega}{(39 + 3.9)\,K\Omega} = 3.545\,K\Omega$$

$$V_{Th} = \frac{V_{CC} R_2}{R_1 + R_2} = 22 \left(\frac{3.9}{3.9 + 39} \right) = 2$$

$\therefore V_{Th} = 2V$

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$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1+\beta) R_E}$$

$$I_B = \frac{2 - 0.7}{3.545 \times 10^3 + (1+100) 1.5 \times 10^3}$$

$$= \frac{1.3}{(3.545 \times 10^3 + 101 \times 1.5 \times 10^3)}$$

$$= \frac{1.3}{(3.545 \times 10^3 + 151.5 \times 10^3)}$$

$$= \frac{1.3}{(3.545 + 151.5) 10^3}$$

$$= \frac{1.3}{155.045 \times 10^3}$$

$$= 8.384 \times 10^{-6} \text{ Amp}$$

$$= 8.384 \text{ le amp}$$

$$I_C = \beta I_B$$

$$= 100 (8.384 \times 10^{-6} \text{ Amp})$$

$$= 8.384 \times 10^{-4} \text{ Amp}$$

$$= 8384 \text{ le Amp}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 22 - 8.384 \times 10^{-4} (10 \times 10^3 + 1.5 \times 10^3)$$

$$= 22 - (8.384 \times 10^{-4} \times 11.5 \times 10^3)$$

$$= 22 - (8.384 \times 11.5 \times 10^{-1}) = 12.3998 \text{ V}$$

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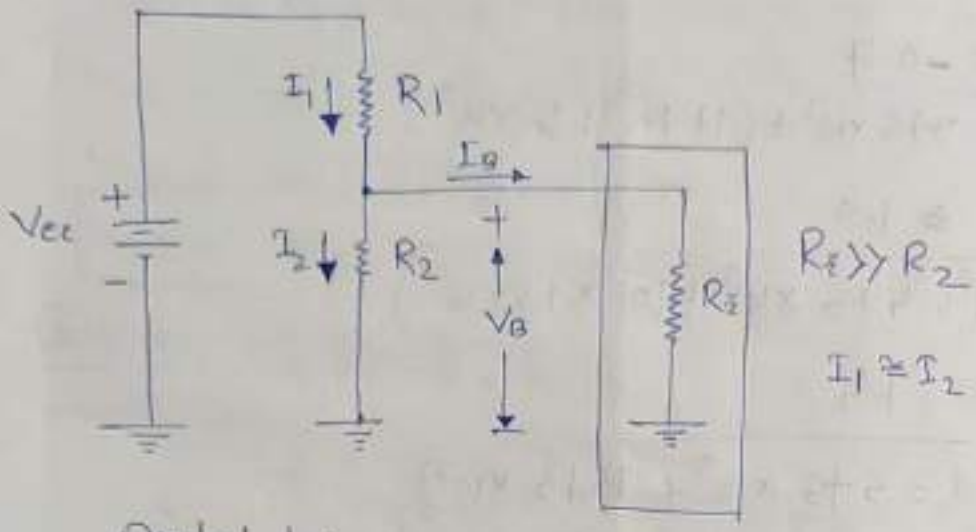
Assignment Approximate Model:



Partial bias circuit for Calculating the approximate base voltage V_B.

The input section of the voltage-divider configuration can be represented by the network of the above fig.

The resistance R_E is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E.

$$R_E = (\beta + 1) R_E$$

If R_E is much larger than the resistance R_2, the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal I_1.

If we accept the approximation that I_B is essentially 0 A compared to I_1 or I_2, and R_1 and R_2 can be considered that the I_B is essentially 0 A can considered series elements. The voltage across R_2, which is actually the base voltage, can be

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determined using the voltage-divider rule, that is

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$R_i = (\beta + 1) R_E \cong \beta R_E$, the condition that will define whether the approximate approach can be applied is:

$$\beta R_E \geq 10 R_2$$

In other words, if β times the value of R_E is at least 10 times the value of R_2, the approximate approach can be applied with a high degree of accuracy.

Once V_B is determined, the level of V_E can be calculated from

$$V_E = V_B - V_{BE}$$

and the Emitter current can be determined.

$$I_E = \frac{V_E}{R_E}$$

and

$$I_{C_Q} \cong I_E$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but because $I_E \cong I_C$

$$V_{CE_Q} = V_{CC} - I_C (R_C + R_E)$$

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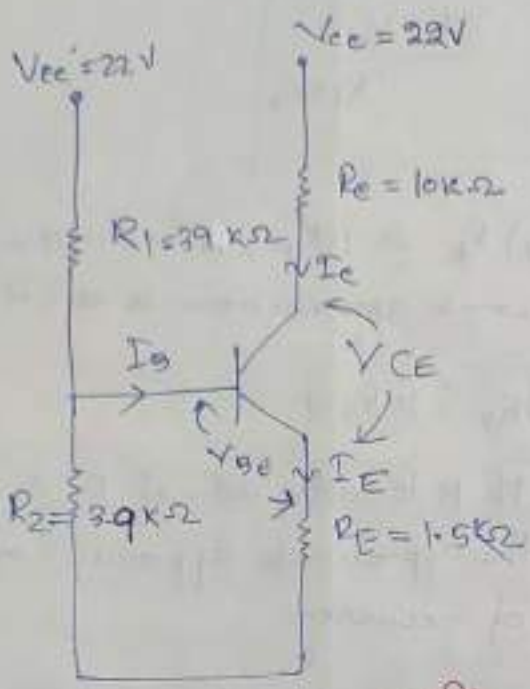
Date: 18/10/19

Problem:



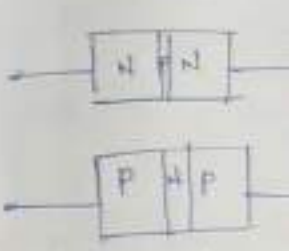
Boylestad Page 182 & 183 11th Edition Example 4.9

Thermal Runaway

The self destruction

Thermal runaway

$\Uparrow I_C = \beta I_B$



Bias Stabilization

Bias stabilization

The process

Q-Point

Variation

Boylestad Page 182, 183 : 11th Edition Example 4.9

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Thermal Runway in transistor:

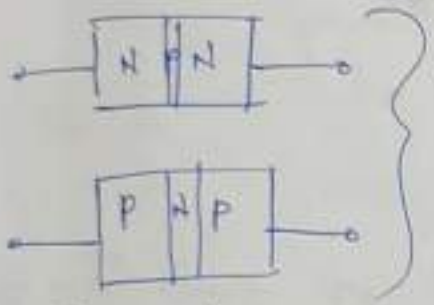
The self destruction of unstabilized transistor is known as Thermal runway.

$\uparrow I_c = \beta I_B + (\beta+1) I_{CBO} \uparrow$ (from the common Emitter configuration)

$\Downarrow$

The temprature is depends on reverse leakage current (I_{CBO})

$\Downarrow$



If it is P type material (electrons are Minority charge carriers)

" " N " " (holes)

Bias Stabilization:

Bias stability & Stability factor:

Stabilization:

The process of making Operating point or Quisent point or Q-Point is independent of temprature changes and variation in transistor parameters. is known as Stabilization.

Q $\Rightarrow$ independent of temp. as well as transistor Parameters (β, I_B, V_{BE})

O/p Q point

I_C & V_{CE}

I/p Q point

I_B & V_{BE}

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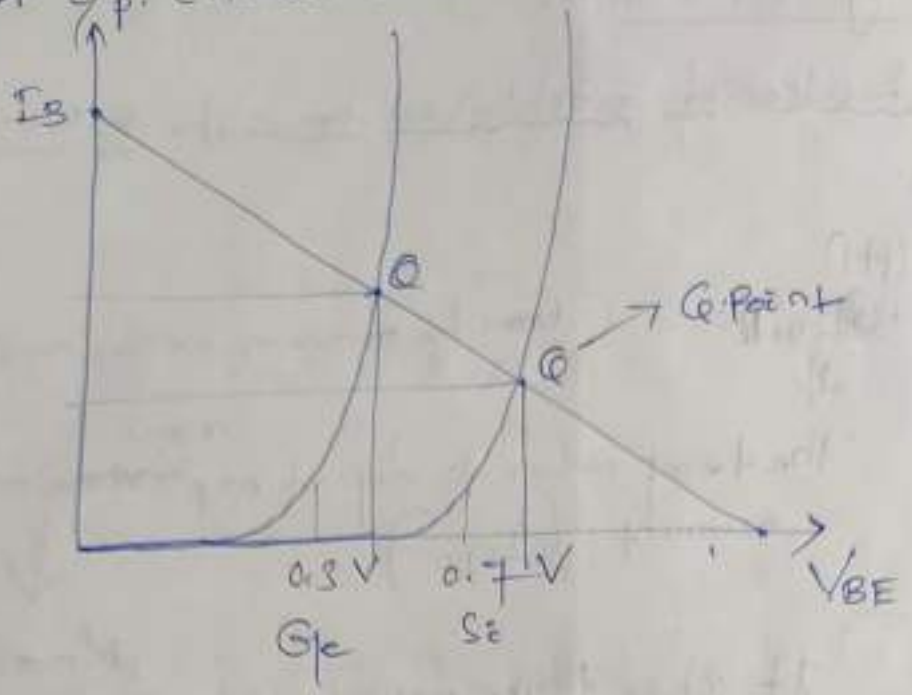
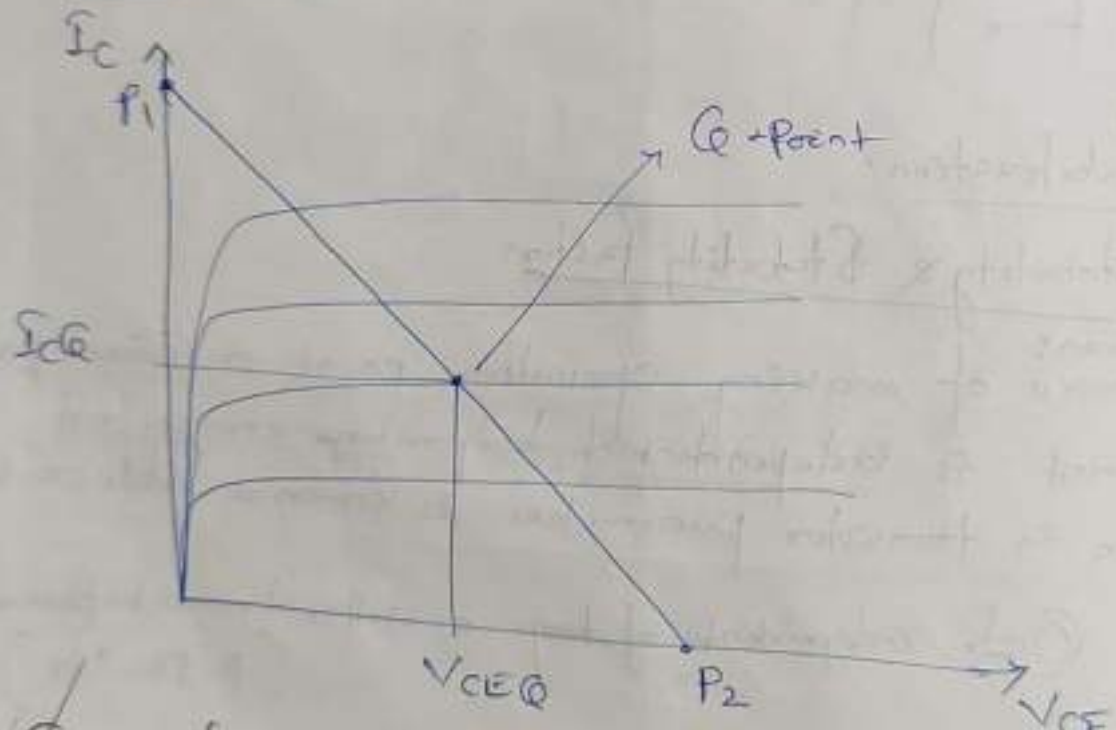
for i/p. characteristics



for o/p characteristics.



Causes of constabilization:

$\uparrow\downarrow I_e = \beta I_B + (\beta+1) I_{CBO}$

$\uparrow\downarrow \propto \uparrow\downarrow V_{CE}$

(i) The Collector current I_C will change of β will change

i.e. $\uparrow I_C \leftarrow \beta \uparrow$

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(ii) The Collector Cunt (I_C) will change if I_{CBO} will change (with I_{CBO} will change when temp will change)

ie. $I_C \propto I_{CBO}$ ⇕

T ⇕ $\propto I_{CBO}$ ⇕

(iii) The change in temprature will also change in input voltage V_{BE}.

(iv) for every 10°c temp change (rise) double the I_{CBO}.

Generally: $I_{CBO} = 0.02$ ↑

ie. 10°c ↑↑ ⇒ $0.02\ (2) = 0.04$
$0.04\ (2) = 0.08$

(v) for Every 1°c temp increase decrease 2.5mV in V_{BE}.

(iv) when I_B ⇕ $\propto I_C$ ⇕

Stability factor: (Stabelization factor)

The rate of change of Collector current (I_C) with respect to reverse leakage current (I_{CBO}) at constant input voltage V_{BE} and amplification factor

$$S = \left.\frac{\partial I_C}{\partial I_{CBO}}\right|_{\text{at } V_{BE} \text{ \& } \beta \text{ constant}} = S(I_{CBO})$$

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Defn: S' The rate of change of Collector current with respect to ~~reverse leakage cu~~ input voltage (V_{BE}) at constant amplification factor (β) and constant reverse leakage current. (I_{CBO}).

$$S' = \left.\frac{d\,I_C}{d\,V_{BE}}\right| \text{ at } \beta \& I_{CBO} \text{ constant} = S(V_{BE})$$

Defn: S'' The rate of change of Collector current with respect to amplification factor (β) at Constant reverse leakage Current (I_{CBO}) and constant input voltage (V_{BE}).

$$S'' = \left.\frac{d\,I_C}{d\beta}\right| \text{ at } V_{BE} \& I_{CBO} \text{ Constant} = S(\beta)$$

NOTE:

1. If 'S' is less then the system is more stable.

eg. $S = 25$

$S = 5$ (More stable system)

Stabilization Factor for fixed bias Configuration:

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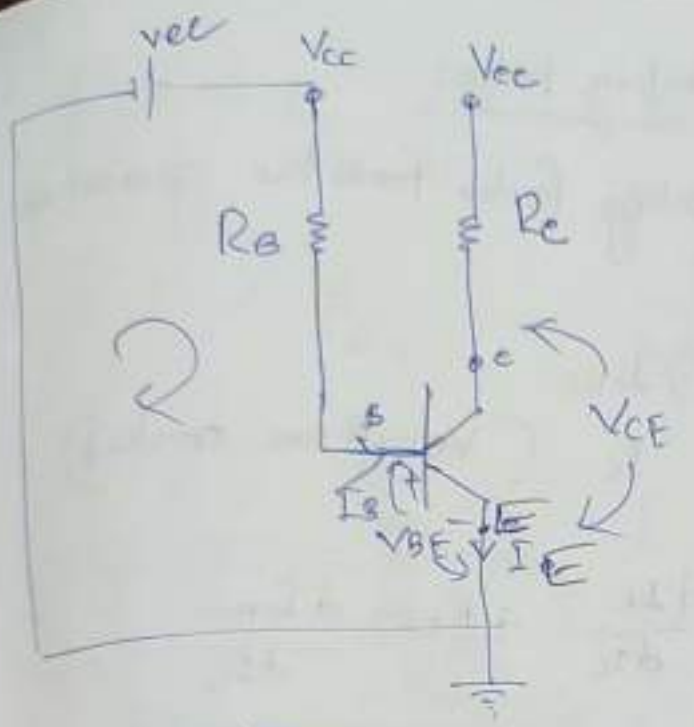

KVL at loop 1,

Step-1 $-V_{cc} + I_B R_B + V_{BE} = 0$ $\quad I_B = \frac{V_{cc} - V_{BE}}{R_B}$ —— (1)

Step-2 $I_C = \beta I_B + (\beta+1) I_{CBO}$

$I_C = \beta \left(\frac{V_{cc} - V_{BE}}{R_B} \right) + (\beta+1) I_{CBO}$ —— (3)

Step-3 Differentiate eqn (3) w.r.t I_C

$$\frac{dI_C}{dI_C} = \frac{\beta}{R_B} \left(\frac{d}{dI_C}(V_{cc} - V_{BE}) + (\beta+1) \frac{d}{dI_C} I_{CBO} \right)$$

(V_{cc} and V_{BE} are constant, so their derivatives are 0)

$$\therefore \quad 1 = \frac{\beta}{R_B}(0-0) + (\beta+1) \frac{dI_{CBO}}{dI_C}$$

$$\Rightarrow \quad 1 = (\beta+1) \frac{1}{S}$$

$$\Rightarrow \quad S = (\beta+1)$$

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Generalized Expression of stability factor:

We can find stability factor from the generalize expression.

$$I_c = \beta I_B + (\beta+1) I_{CBO}$$

differentiate w.r.t I_c (V_{BE}, β are constant)

$$\frac{dI_c}{dI_c} = \beta \frac{dI_B}{dI_c} + (\beta+1) \frac{dI_{CBO}}{dI_c}$$

$$1 = \beta \frac{dI_B}{dI_c} + (\beta+1) \frac{1}{S}$$

$$\left(1 - \beta \frac{dI_B}{dI_c}\right) = (\beta+1) \frac{1}{S}$$

$$S = \frac{(\beta+1)}{\left(1 - \beta \frac{dI_B}{dI_c}\right)}$$

$$S = \frac{dI_c}{dI_{CBO}}$$

$$\frac{1}{S} = \frac{dI_{CBO}}{dI_c}$$

$$\frac{dI_B}{dI_c} = 0$$

($\because I_B$ is independent of I_{CBO}, I_B is constant here)

$$S = \frac{\beta+1}{1} = \beta+1$$

$$S' = \frac{dI_c}{dV_{BE}}$$ at β and I_{CBO} constant

$$I_c = \beta \left(\frac{V_{cc} - V_{BE}}{R_B}\right) + (\beta+1) I_{CBO}$$

Now, differentiate w.r.t I_c (β, I_{CBO} constant)

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$$\frac{dI_c}{dI_c} = \frac{\beta}{R_B}\frac{d}{dI_c}(V_{cc} - V_{BE}) + (\beta+1)\frac{dI_{cBo}}{dI_c}$$

0

$$1 = \frac{\beta}{R_B}\left(0 - \frac{dV_{BE}}{dI_c}\right) + 0$$

$$1 = \frac{\beta}{R_B}\left(-\frac{1}{S'}\right) \qquad \left(\because \frac{1}{S'} = \frac{dV_{BE}}{dI_c}\right)$$

$$S' = \frac{-\beta}{R_B}$$

Assignment S'':

$$S'' = \left.\frac{dI_C}{d\beta}\right|_{\text{at } V_{BE} + I_{cBo} \text{ constant}} = S_\beta)$$

$$I_C = \beta I_B + (\beta+1) I_{CO}$$

Substituting I_B in the above eqn.

$$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right) + (\beta+1) I_{CO}$$

$$= \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta+1) I_{CO}$$

Differentiating the above equation with respect to β

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B} + I_{CO}$$

$$= I_B + I_{CO}$$

$$\cong I_B$$

$$\Rightarrow \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta} \Rightarrow \boxed{S_\beta = I_C/\beta}$$

refer. Analog electronic ckt Sample paper, Pg 11 Q12

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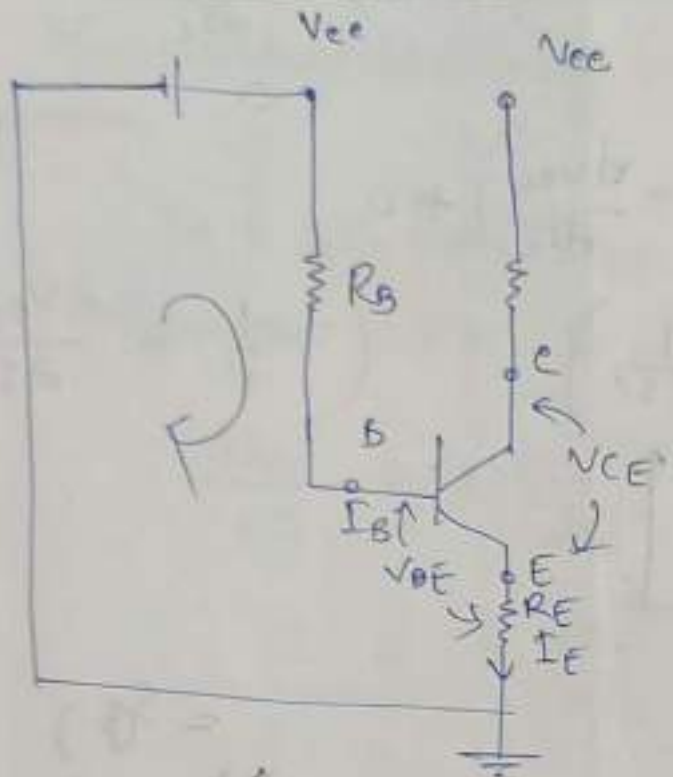
Stabilization factor for Emitter bias Configuration:



Step 1 Applying KVL:

$+V_{cc} - I_B R_B - V_{BE} - I_E R_E = 0$

$I_E = I_C + I_B$

$V_{cc} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0$

$V_{cc} - I_B R_B - V_{BE} - I_C R_E - I_B R_E = 0$

$V_{cc} - I_B (R_B + R_E) - V_{BE} - I_C R_E = 0$

Step 2

$$I_B = \frac{V_{cc} - V_{BE} - I_C R_E}{R_B + R_E} \quad \text{---(1)}$$

Step-2

$I_C = \beta I_B + (\beta + 1) I_{CBO}$

$$I_C = \beta \left(\frac{V_{cc} - V_{BE} - I_C R_E}{R_B + R_E} \right) + (\beta + 1) I_{CBO} \quad \text{---(2)}$$

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Step 3: Differentiating partially respect to I_C (V_{BE} & β constant)

$$\frac{dI_C}{dI_C} = \frac{\beta}{R_B+R_E}\frac{d}{dI_C}\left(V_{CC}^{0} - V_{BE}^{0} - I_C R_E\right) + (\beta+1)\frac{dI_{CBO}}{dI_C}$$

$$1 = \frac{\beta}{R_B+R_E}\left(-\frac{d}{dI_C} I_C R_E\right) + \frac{\beta+1}{S}$$

$$1 = \frac{\beta}{R_B+R_E}\times(-R_E) + \frac{\beta+1}{S}$$

$$1 = -\frac{\beta R_E}{R_B+R_E} + \frac{\beta+1}{S}$$

$$\left(1+\frac{\beta R_E}{R_B+R_E}\right) = \frac{\beta+1}{S}$$

$$S = \frac{\beta+1}{\left(1+\frac{\beta R_E}{R_B+R_E}\right)} = \frac{\beta+1}{\frac{R_B+R_E+\beta R_E}{(R_B+R_E)}}$$

$$= \frac{(\beta+1)(R_B+R_E)}{R_E(1+\beta)+R_B}$$

$$\therefore S = \frac{(\beta+1)(R_E+R_E')}{R_E(1+\beta)+R_B}$$

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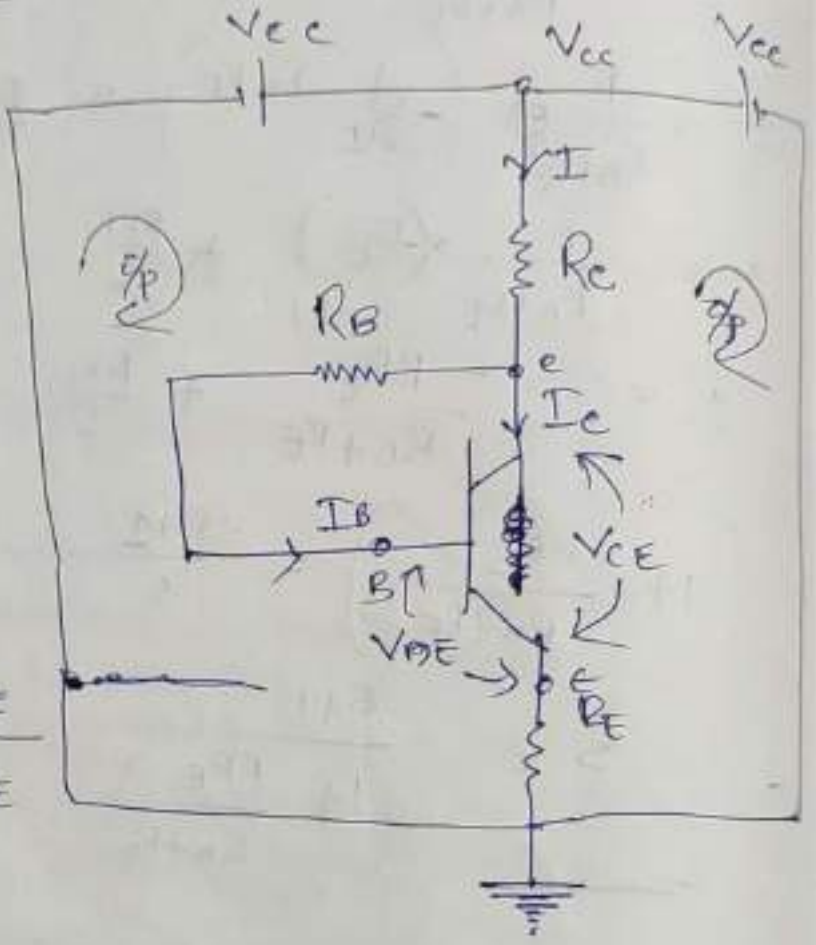
Date 22/10/19

Stabilization factor for Collector feedback biasing Configuration.

With Emitter Resistance



KVL & KCL,

$I = I_c + I_B$

$I_B = ?$

$I_c = ?$

$R_E = ?$

KVL,

$$I_B = \frac{V_{cc} - I_c R_E - V_{BE}}{R_E + R_E}$$

Apply KVL

$$V_{cc} - I_B R_c - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\Rightarrow V_{cc} - V_{BE} = I_B R_c + I_B R_B + I_E R_E$$

$$\Rightarrow = (I_B + I_c) R_c + I_B R_B + I_E R_E$$

$$V_{cc} - V_{BE} = R_c I_B + I_c R_c + I_B R_E + I_E R_E$$

$$\Rightarrow V_{cc} - V_{BE} = I_B (R_c + R_E) + I_c R_c$$

$$\Rightarrow \frac{V_{cc} - V_{BE} - I_c R_c - I_E R_E}{R_c + R_E} = I_B$$

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$I_C = \beta I_B + (\beta+1) I_{CBO}$

$I_C = \beta \left(\frac{V_{CC} - V_{BE} - I_C R_C - I_E R_E}{(R_C + R_E)} \right) + \left(\frac{V_{CC} - V_{BE} - I_C R_C - I_E R_E}{R_C + R_E} \right) I_{CBO}$

$I_C =$

$S =$

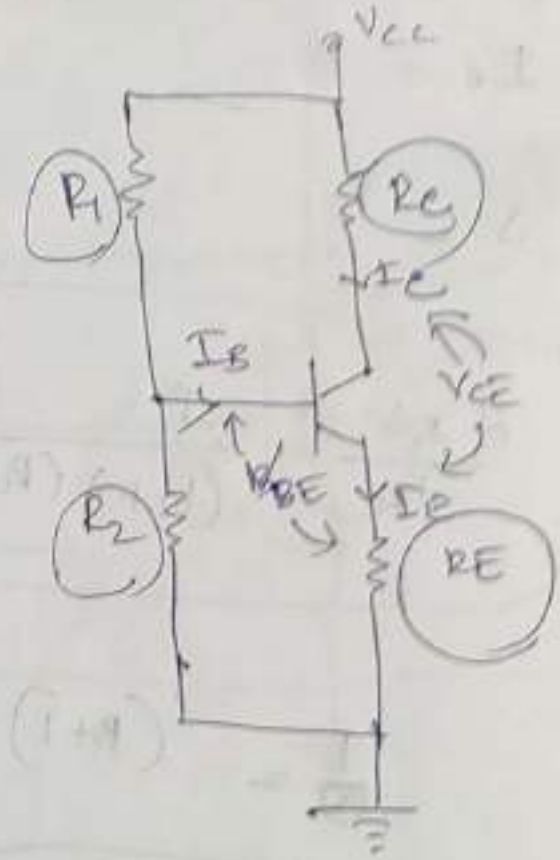
$$\frac{dI_C}{dI_C} = \frac{\beta}{(1+\beta)(R_C+R_E)+R_B} \frac{d}{dI} (V_{CC} - V_{BE}) + (\beta+1) \frac{dI_{CBO}}{dI_C}$$

$$\frac{1}{S} = (\beta+1) \frac{1}{S}$$

$$S = 1 + \beta$$

Problem: design a "voltage divider bias network" using a supply voltage of 24V, a transistor with $\beta = 110$, and operating points of $I_{CQ} = 4mA$ and $V_{CEQ} = 8V$, Choose $V_E = \frac{1}{8} V_{CC}$.

Solution:



$V_{CC} = 24\ V$

$\beta = 110$

$I_{CQ} = 4mA$

$V_{CEQ} = 8V$

$V_E = \frac{1}{8} V_{CC}$

R_1, R_2, R_C, R_E

$I_C = \beta I_B$

$4mA = 110 (\quad$

(1) $R_E = ?$

$I_C \approx I_E$

$$R_E = \frac{V_E}{I_E} = \frac{V_E}{I_C}$$

$V_E = \frac{1}{8} V_{CC}$

$V_E = \frac{24}{8} = 3V$

$V_E \approx 3V$

$R_E = \frac{3}{4 \times 10^{-3}}$

$= 0.75\ K\Omega$

R_2

(ii) $R_c = \frac{V_c}{I_C}$

$V_{CE} = V_c - V_E$

$\Rightarrow V_c = V_{CE} + V_E$

$= 8V + 3V$

$V_c = 11V$

$R_c = \frac{11}{4 \times 10^{-3}} = 2.75 K\Omega$

(iii) for approximate analysis

$\beta R_E \geq 10 R_2$

$\beta R_E = \beta R_2$

$\frac{\beta R_E}{10}$

~~$R_2 = \frac{10}{\beta R_E} = \frac{10}{110 \times 0.75 \times 10^3}$~~

$R_2 = \frac{110 \times 0.75 \times 10^3}{10}$

$R_2 = 8.25 K\Omega$

~~$R_1 + R_2$~~ $\cdot V_2 = V_B = \frac{R_2 (V_{CC})}{R_1 + R_2}$

$V_{BE} = V_B - V_E$

$V_B = V_{BE} + V_E$

$= 0.7V + 3V = 3.7V$

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$$V_B = \frac{(8.25\,K\Omega)(1+V)}{R_1 + (8.25\,K\Omega)}$$

$$3+V(R_1 + 8.25\,K\Omega) = (8.25\,K\Omega \times 29\,V)$$

$$R_1 \times 3.7 = (8.25\,K\Omega \times 27) - (8.25\,K\Omega)$$

$$R_1 = 9.583\,K\Omega$$

$$R_1 = 2223.27\,\Omega$$

$$= 2.223\,K\Omega$$

for the desiding of voltage, devided base configuration

$R_1 = 45.28\,K\Omega$

$R_2 = 8.25\,K\Omega$

$R_e = 2.75\,K\Omega$

$R_E = 0.75\,K\Omega$

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FET (Field Effect Transistor)

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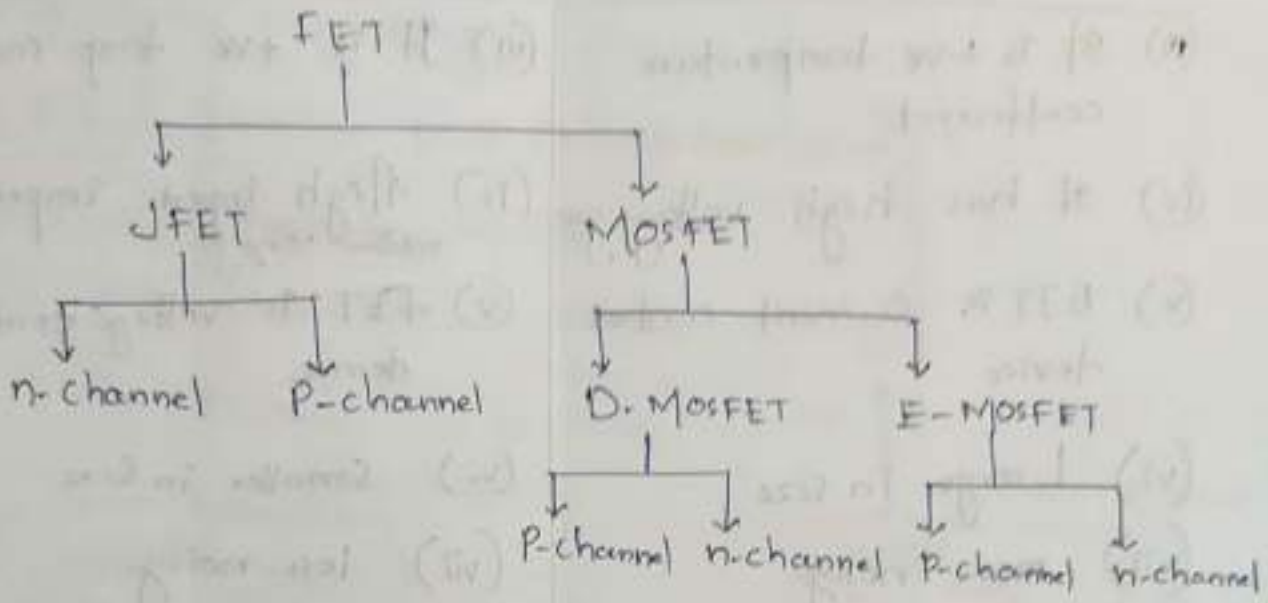
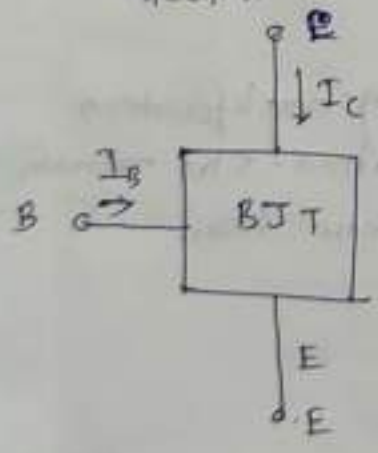
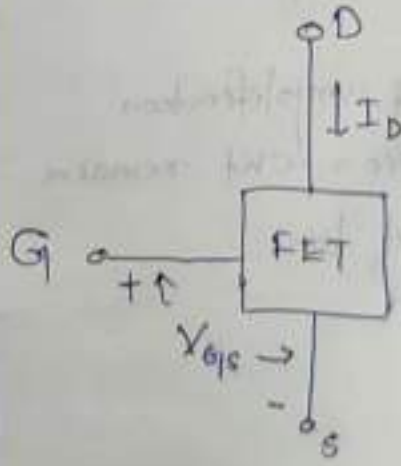


* Difference betn BJT and FET:

BJT (Bipolar Junction Transistor)	FET (Field Effect transistor)
(i) BJT is 3 terminal device. These are Emitter, Base & Collector. 	(i) FET is 3 terminal device Gate, Source and Drain. 
(ii) Bipolar junction transistor means conduction takes place because of both holes & electrons.	(ii) Unipolar junction transistor. because conduction of current takes place either by holes or electrons.

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BJT (Bepolar Junction Transistor)	FET (field Effect transistor)
(iii) It is -ve temprature coeffecient.	(iii) It is +ve temp coeffecient
(iv) It has high voltage gain	(iv) High input impedance
(v) BJT is current control device	(v) FET is voltage control device
(vi) Large in size	(vi) Smaller in size
(vii) more noisy	(vii) less noisy
(viii) Small current is required to keep the device on	(viii) Small voltage is required to keep the device on
(ix) less Thermal Stable	(ix) Thermal Stable.
(x) Mainly BJT are of 2 types (i) npn (ii) pnp	(x) Mainly FET are of 2 types (i) JFET (ii) MOSFET
(xi) During amplification operation ckt remains forward bias.	(xi) During amplification operation ckt remain reverse bias.

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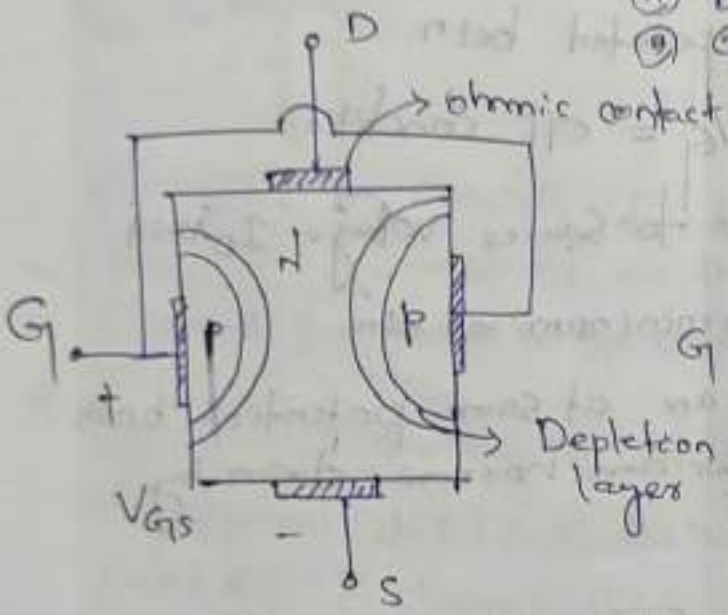
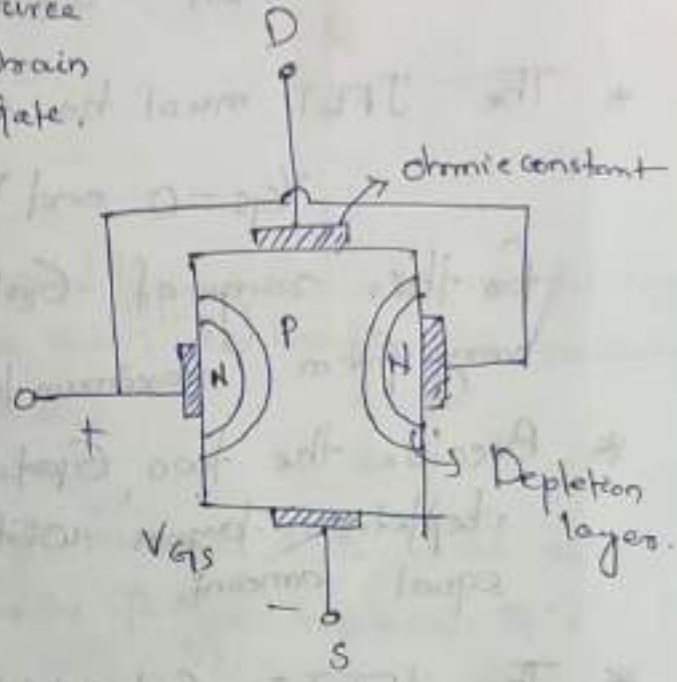
Similarities both BJT & FET:

* Both will use amplifier switching device and impedance matching.

JFET (Junction feeld Effect transistor):

* It is a 3 terminal device
* The 3 terminal are, ① Source ② Drain ③ Gate.





2 type of FET:

① n-channel
② P-channel

*** N-channel JFET is widely used

* It is a 3 terminal voltage control semiconductor device
* That means input voltage controls output characteristics of JFET.

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* JFET is always operated with Gate to source
* PN Junction is reverse bias.
* In FET Gate Current (I_G) is zero.

  ie $I_G = 0$

  Sence there is no Gate current.

  then $I_D = I_S$.

* The JFET must be operated betn

  $V_{GS} = 0$ and V_G = off condition.

  for this range of Gate to Source voltage I_D will vary from maximum to minimum of zero.
* Because the two Gate are at same potential both depletion layers wider and narrow down by equal amount.
* The JFET is Subjected to Thermal runaway effect when the temprature of device increases.
* The I_D is controlled by changing in the Channel

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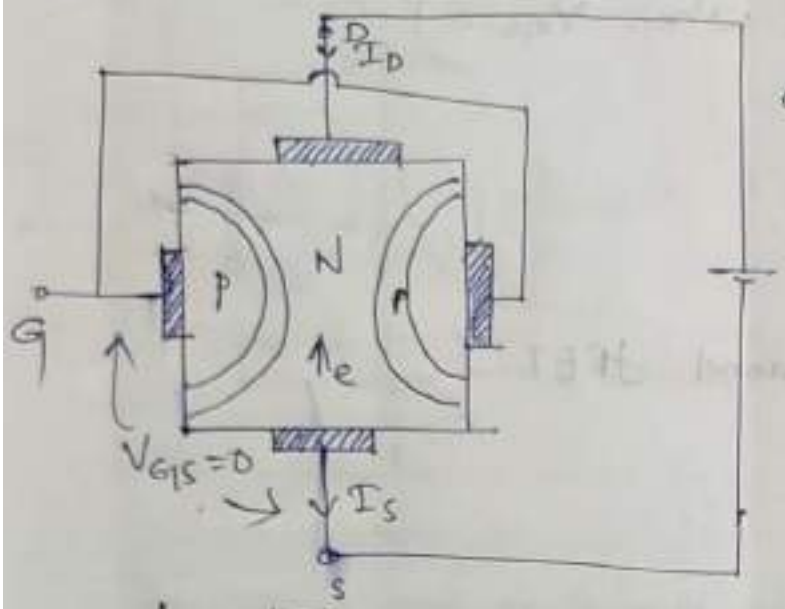
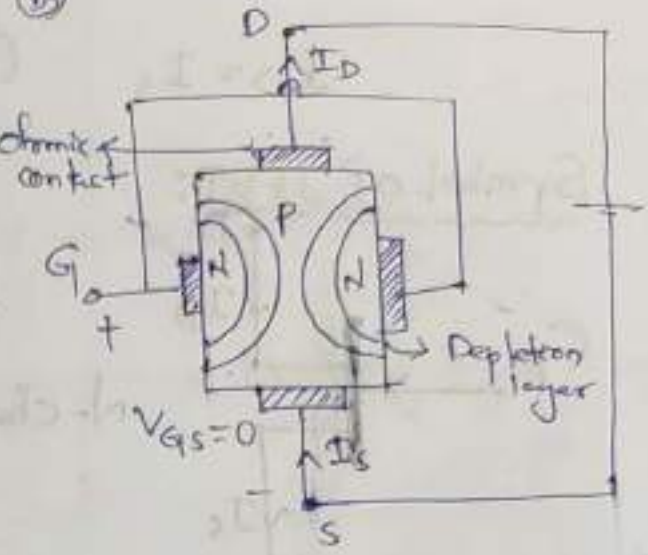
Construction of JFET:

(a) N-channel JFET:



(b) P-channel JFET:



A JFET consists of a P or N type Silicon bar containing two PN-Junctions at the sides. The bar forms the conducting channel for the charge carriers.

* NOTE: If the bar is N-type material it is called as N-channel JFET & if the bar is P-type material it is called as P-channel JFET.

* The two PN-Junction forming diodes are connected internally at a common terminal called Gate.

* Other terminals are Source and drain taken out from the either channel.

* Thus a JFET has 3 terminals - Called Source, Gate & Drain.

JFET Polarities:

* The input ckt of JFET is reverse biased this means that devices has high input impedance

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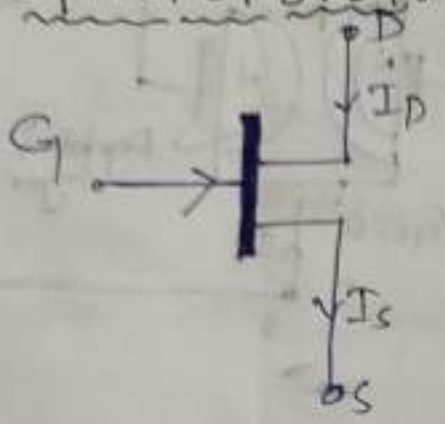
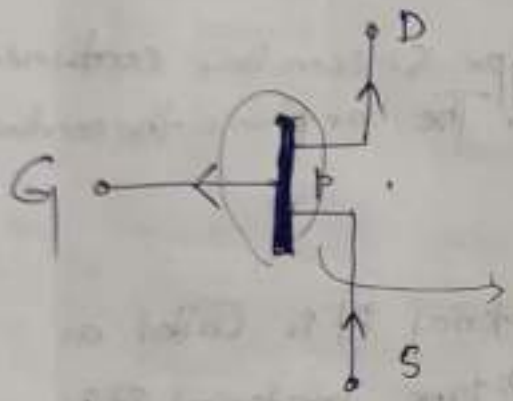
* The drain is biased w.r.t the source.

$I_D = I_S$ (when $V_{GS}=0$)

Symbol of JFET:



N-channel JFET



P channel JFET

Gate is thick because p region is more comparable to N.

WORKING OF JFET: (Operating Principle)

Case 1: $V_{GS}=0$

Case 2: $V_{GS}<0$

} $V_{DS} > 0V$

Condition 1: ($V_{GS}=0$, $V_{DS}>0V$)

* The two PN-Junction at the side forms two depletion layers the current conduction by charge carriers i.e. electrons in case of N-channel and hole in case of P-channel.

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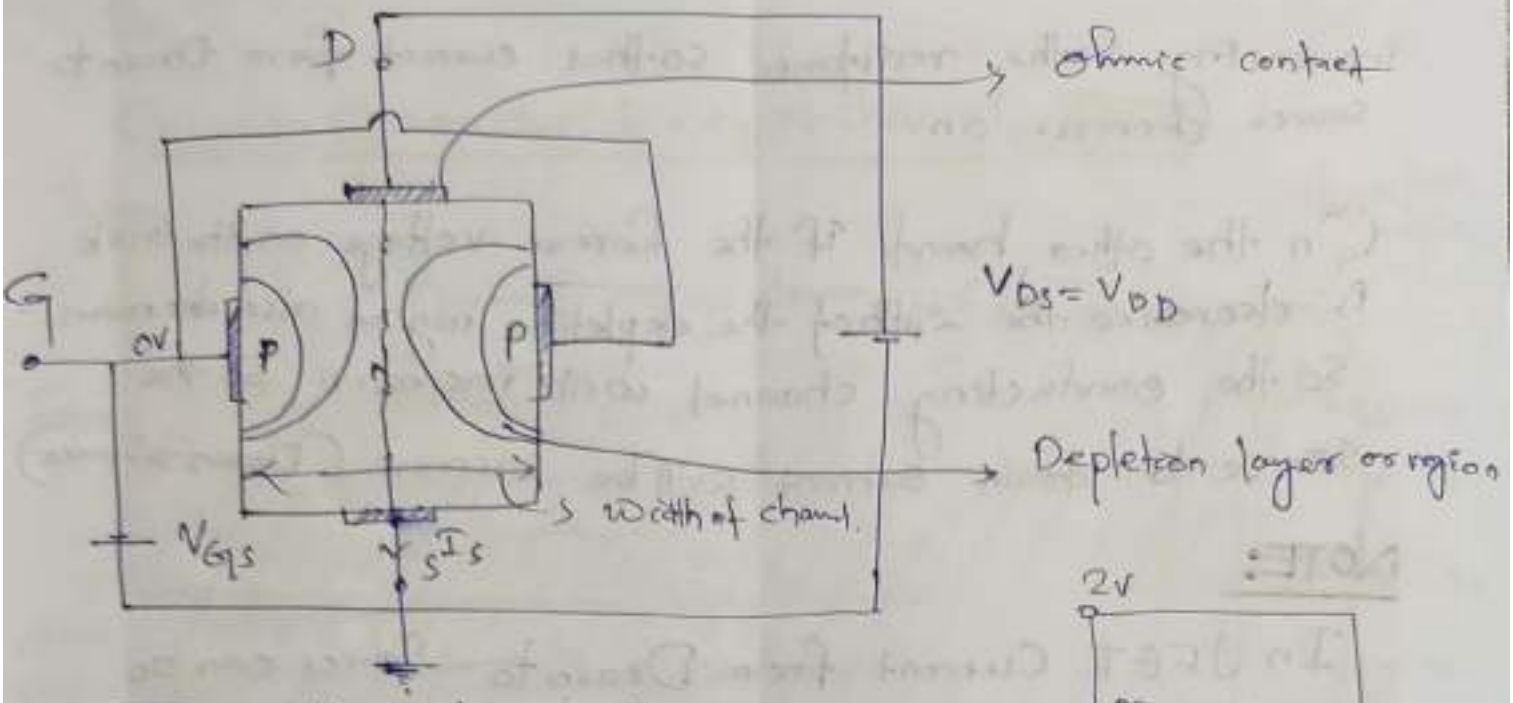

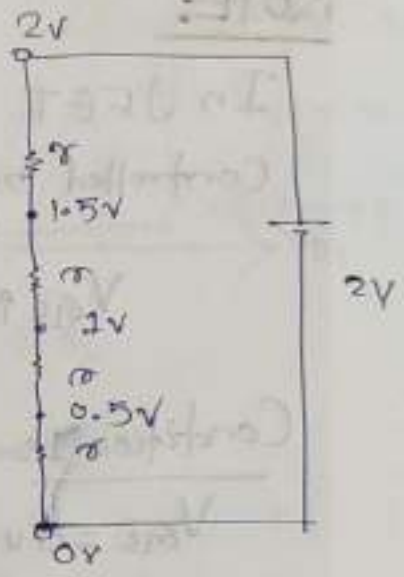

The width and resistance of the channel can be control by changing the input voltage V_{GS}.

The greater the reverse voltage V_{GS}. The wider will be the depletion layer & narrow the channel.

JFET operate on the principle that width and resistance of conducting channel can be varied by changing V_{GS}.

WORKING:

When a voltage V_{DS} is applied both source and drain and the voltage on the Gate is zero. The PN-Junction at the side of the bar has establi- depletion layer.

The size of the depletion layer determine the width of the channel and hence current conducts through the bar.

When a reverse voltage V_{GS} is applied both Gate & source the width of the depletion layer is increased this reduces the width of the conducting channel. Thereby

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increasing in the resistance so that current from Drain to Source decrease.

On the other hand if the Reverse voltage on the Gate is decreases the width of the depletion region also decreases so the conducting channel will increases. So the source to drain current will be increase. (Drain to Source)

NOTE:

In JFET Current from Drain to Source can be Controlled by applying potential across Gate terminal

$V_{GS}\uparrow$ DL $\uparrow$ Channel W $\downarrow$ Source to Drain $\downarrow$

Condition 1:

$V_{GS} = 0v$, $V_{DS} > 0$, $I_D = I_S$

Condition 2:

$V_{GS} < 0$, $V_{DS} > 0$, $I_D > I_S$

Pinch off Voltage:-

Pinch off voltage is the drain to source voltage after which the Drain to source current becomes almost constant JFET enters into saturation region it is defined only when Gate to source voltage will be zero.

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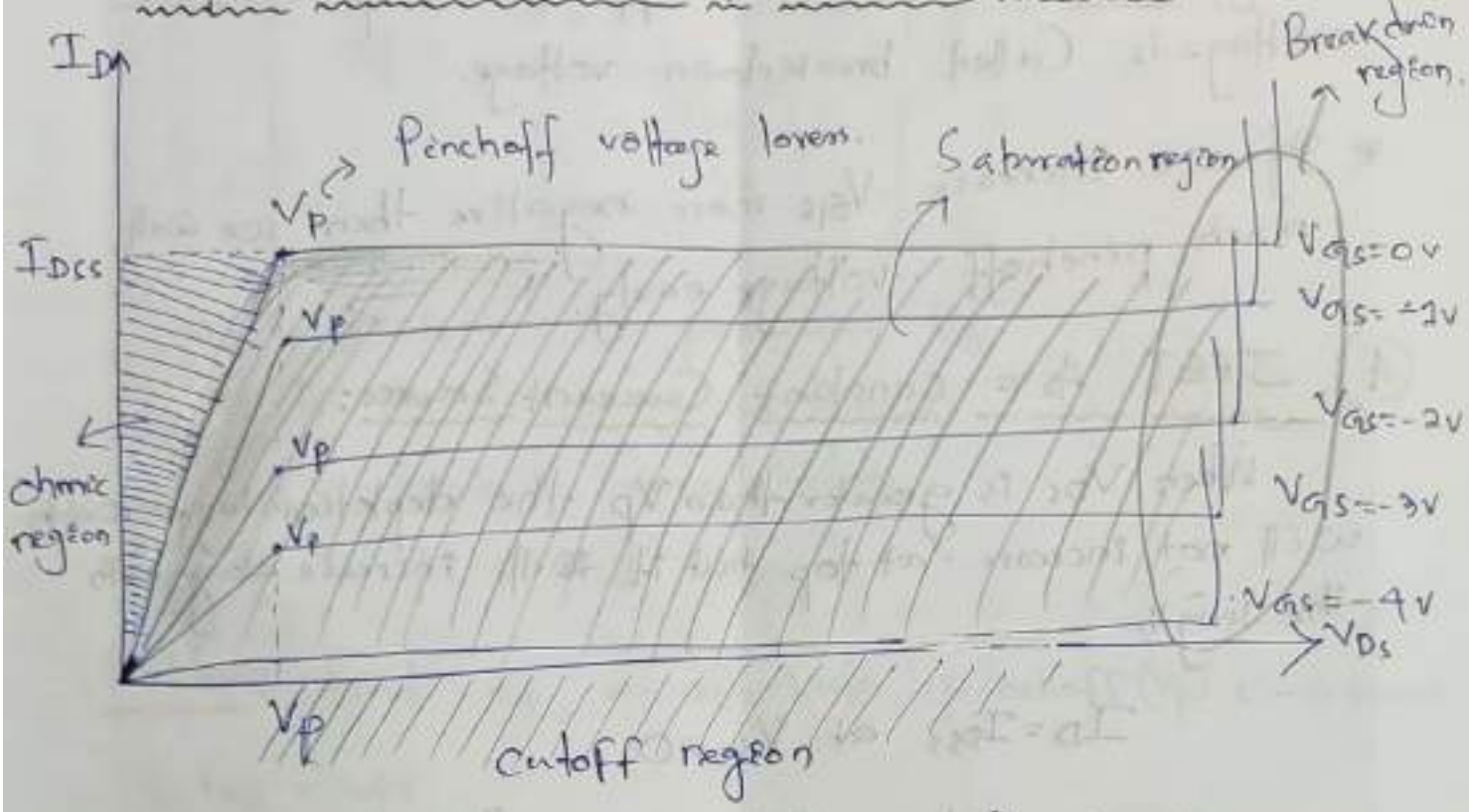
Output characteristics of N-channel JFET:



$I_D = I_{DSS}$ = Maximum Saturation Current.

* It is the graph betn I_D versus V_{DS} at Constant V_{GS}.
* The drain current (I_D) rises linearly with drain to source voltage V_{DS} then I_D becomes constant.
* The drain to source voltage (V_{DS}) above which drain current becomes constant at pinchoff voltage V_p.

After V_p the channel width becomes so much narrow the depletion layer almost touches each other the I_D passes through through the small passage betn thes layers therefore increasing I_d is very small with increase in V_{ds} above pinchoff voltage.

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* If we keepon increases V_{DS} at the some particular voltage breakdown will happen. This particular voltage is Called breakdown voltage.

* If we increase V_{GS} more negative then we will reach pinchoff voltage early.

(A) JFET As a constant Current Source:

When V_{DS} is greater than V_p the depletion layer width will not increase at top but it will increase along with the length

$$I_D = I_{DSS} \text{ at } V_{GS} = 0$$

I_{DSS} = Maxm Saturation Current

If I_D will not increase further at $V_{DS} < V_{DS\,max}$. thats why, JFET acting as constant current soures.

(B) JFET as voltage control resistor:

- Ohmic region is also Called as voltage control resistance region.

NOTE: JFET can use as variable resistor in ohmic region.

$$V_{DS} = I_{DSS}\,(R)\uparrow$$

$$R\uparrow = \frac{1}{\text{Slop}} = \frac{1}{0} = \infty \Big|_{V_{GS}}$$

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for finding the drain resistance:

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$

r_d is resistance at particular V_{GS}

r_o is the resistance at $V_{GS} = 0$

V_{GS} = Gate to Source voltage

V_p = pinch off voltage.

Problem: find r_d, at $r_o = 10K\Omega$, pinchoff$(V_p) = -6V$ and $V_{GS} = -3V$.

Solution:

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$

Given, $r_o = 10K\Omega$

$V_p = -6V$

$V_{GS} = -3V$

$$\therefore r_d = \frac{10K\Omega}{\left[1 - \left(\frac{-3V}{-6V}\right)\right]^2} = 40K\Omega. \quad \text{(Ans)}$$

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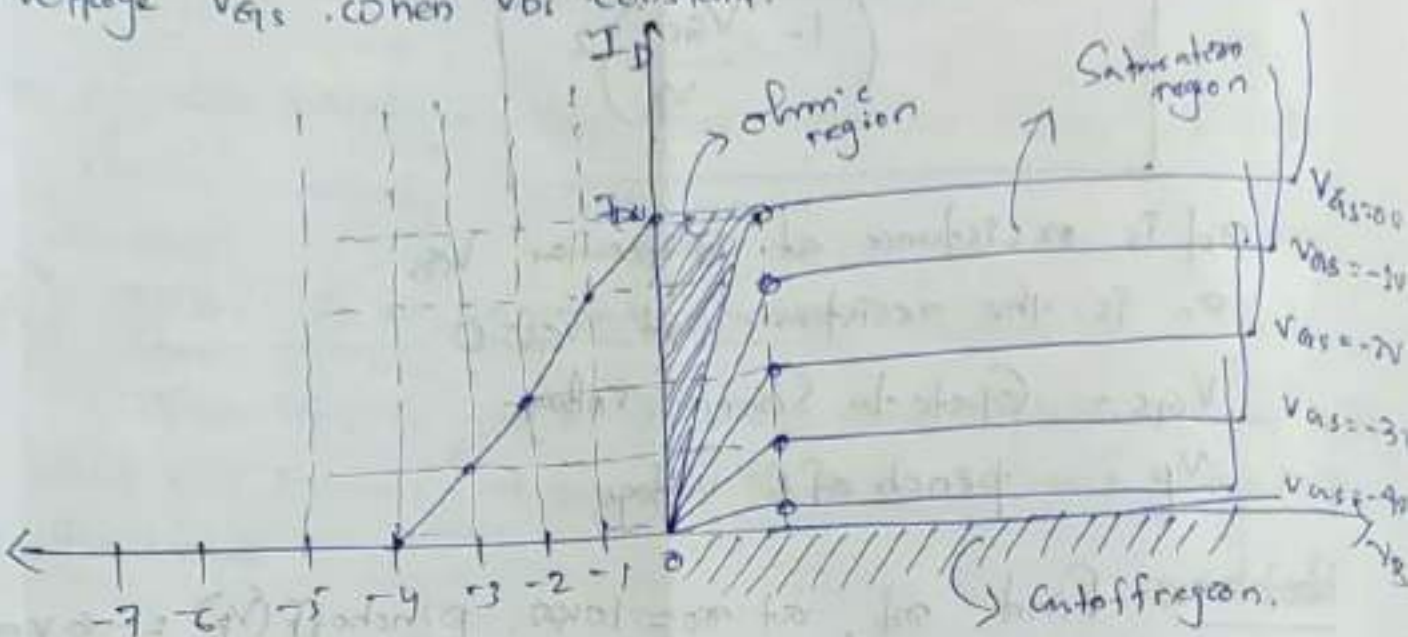
Transfer characteristics of N-channel JFET:

It is the graph betn output Current I_D versus Input voltage V_{GS} when V_{DS} constant.



Schokley's Equation's

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Transconductance (g_m):

Transconductance is defined as the ratio of change in I_D to the change in gate to source voltage at constant drain to source voltage.

i.e. $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ mA/V}$$ at constant V_{DS}

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Amplification factor: (μ)

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

It is the ratio of change in V_{DS} to change in V_{GS}.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D}$$

$$\mu = r_d \times g_m$$

Ac drain Resistance:

It is the ratio of change in (I_D) to change in gate to source voltage at constant drain to source voltage V_{DS}.

$$R_D (ac) = \frac{I_D}{V_{DS}}$$

Prob① The device parameters for n-channel JFET are

Maxm drain current (I_{DSS}) = 10mA

pinch off voltage (V_p) = $-4V$

Calculate the drain current for

ⓐ $V_{GS} = 0V$, ⓑ $V_{GS} = -1V$ ⓒ $V_{GS} = -4V$.

Solution: Given, $I_{DSS} = 10mA$

$V_p = -4V$

ⓐ $V_{GS} = 0V$

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(a) $V_{GS} = 0V$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$= 10mA\left(1 - \frac{0}{-4}\right)^2$$

$$I_D = 10mA$$

(b) $V_{GS} = -1V$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$= 10mA\left(1 - \left(\frac{-1}{-4}\right)\right)^2$$

$$= 5.625\,mA$$

(c) $V_{GS} = -4V$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$= 10mA\left(1 - \frac{-4}{-4}\right)$$

$$= 0A$$

Problem (2): A JFET produce gate current 2nA when gate is reverse biased with 8V Determine the resistance between gate & source.

Solution: Given $I_G = 2nA$

$V_{GS} = 8V$

$$R_{GS} = \frac{V_{GS}}{I_G} = \frac{8V}{2nA} = 4 \times 10^9 \Omega$$

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Problem ③: The reverse gate voltage of JFET when changes from +1V to +1.2V. The drain current changes from 2.2mA to 2.6mA. Find the value Transconductance (g_m)

Solution:

Given,

change in gate voltage $(\Delta V_{GS}) = (4.4 - 4.2)V = 0.2V$

Change in drain current $(I_D) = 2.2mA - 2.6mA = -0.4mA$

$$g_m \text{ (Transconductance)} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ mA/V}$$

$$= \frac{-0.4}{0.2} = 2 \text{ mA/V or } 2mS$$

Problem ④: The pinchoff voltage for an n-channel JFET is 4V the pinchoff occurs for V_{DS} when $V_{GS} = -1$ volts.

(a) 3 volts (b) 5 volts (c) 4 volts (d) 1 volts.

Solution:

Given, $V_p = 4V$ $I_D = I_{DSS}$

$V_{GS} = -1V$

$V_{DS} = ?$

$$V_p = V_{DS}\Big|_{V_{GS}=0}$$

So, $V_p = V_{DS} = (4-1)\Big|_{V_{GS}=-1}$

$= 3V$

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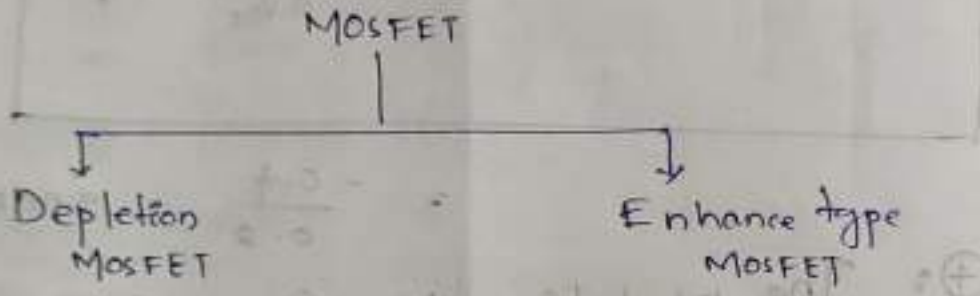
MOSFET

Metal oxide Semiconductor field Effect transistor (MOSFET)

MOSFET is a voltage control device which control the output current (I_D) by input voltage (V_{GS}).

MOSFET has characteristics similar to JFET and additional characteristics that make them very useful.

MOSFET are available in two types.



Depletion type MOSFET (D-MOSFET):

In D-MOSFET there is a physical channel exist bet^n source and drain region and sufficient Gate the source +Ve Potential is applied across gate terminal to form the channel.

It operates in +Ve gate bias condition.

Construction of depletion type MOSFET:

A slab of p-material is form from Silicon base then we will introduces trivalent empurity then we have P type Substrate.

Substrate: Substrate is the base or fundation on which our device is constructed.

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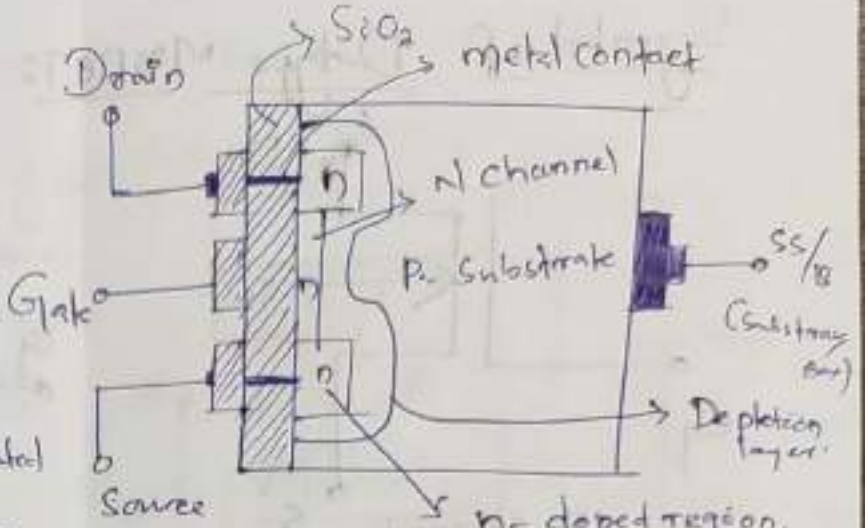
The source and drain are connected through metallic metal contact to N-doped region linked by n-channel.

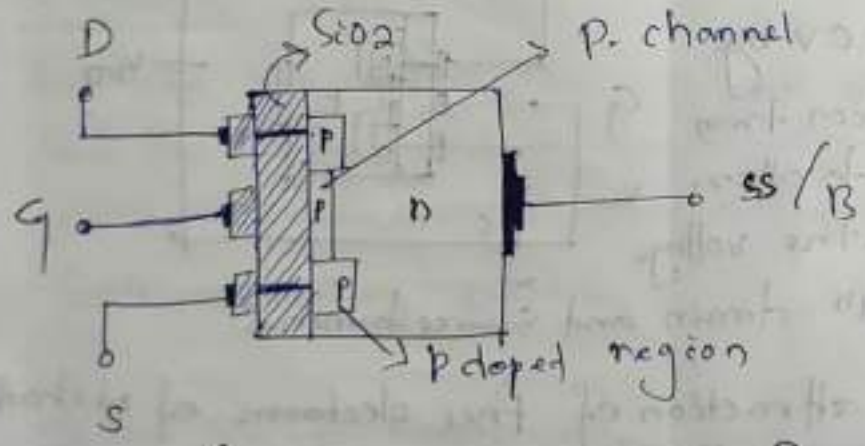
The Gate also connected to metal contact surface insulated from n-channel by a very thin SiO_2 layer.



(fig: N-channel MOSFET)

SiO_2 is type insulating refer to as a dielectric wherein sets of opposing electric field within the dielectric when exposed to an externally applied electric field There is no direct electrical connection betn gate and terminal & channel of MOSFET.

It is the resulting layer of MOSFET that accounts for high input impedance of the device.



(fig: P-channel MOSFET)

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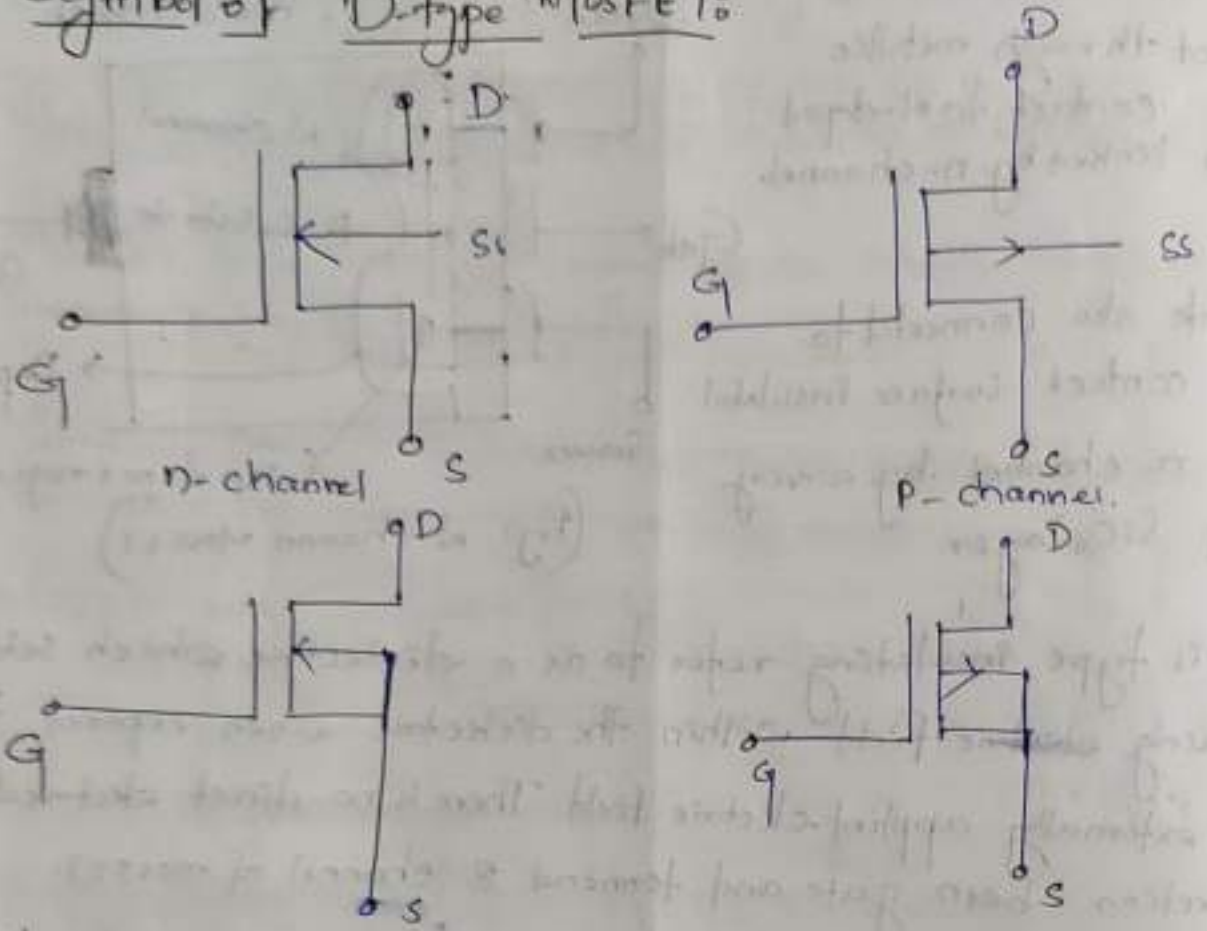
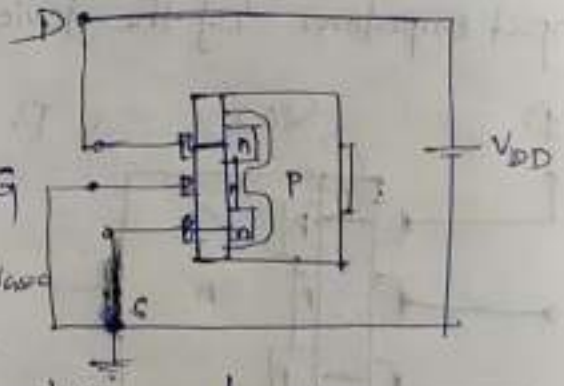
Symbol of D-type MOSFET:



Working Operation of DMOSFET:

Case (1) $V_{GS}=0$:



The V_{GS} is set to 0V by the direct connection from the one terminal to others. ie Gate to source the voltage V_{DD} is applied both drain and source terminal.

- The result is an attraction of free electrons of n channel for the +ve voltage at the drain.

The resulting current decreases equal to zero volt.

$$I_D = I_{DSS}$$

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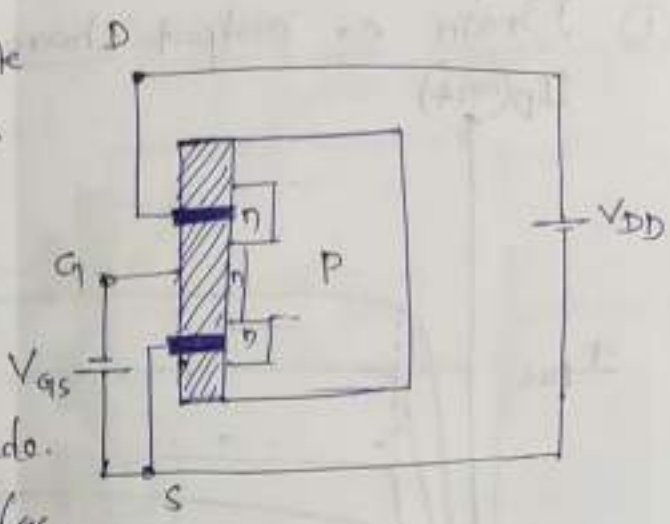
Case (ii): V_{GS} = -Ve voltage

The -Ve potential at the gate will tends to press electrons towards p. substrate & attracts holes from P-type substrate.



Depending upon the magnitude of -Ve bias stablish by V_{GS}.

A level of recombination between electrons holes will occurs that will reduce the no. of free electrons in the n-channel available for conduction.

The more negative bias the higher is the recombination. The resulting level of drain Current is therefore reduce with increase in -Ve bias for V_{GS}.

Case (iii): V_{GS} = +Ve

For +Ve value of V_{GS} the +Ve gate will draw additional electrons from the P-type substrate due to reverse leakage Current and establish new charge carriers through the Collision resulting both accelerating particles.

* As the gate to source voltage continuous to increase in the +Ve direction the I_D will increase at a rapid rate. This is known as enhancement mode of operation of D-MOSFET.

$$I_D \propto V_{GS}$$ at V_{DS} = Constant.

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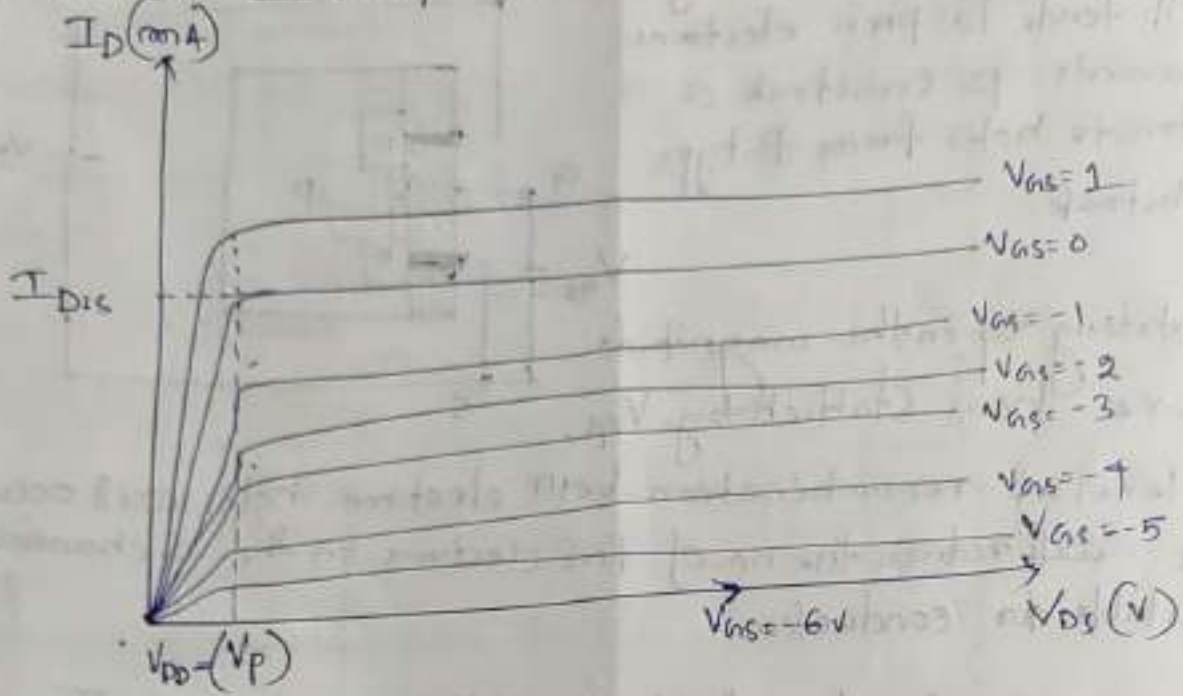
Characteristics of DMOSFET:

① Drain or output characteristics of N-channel DMOSFET

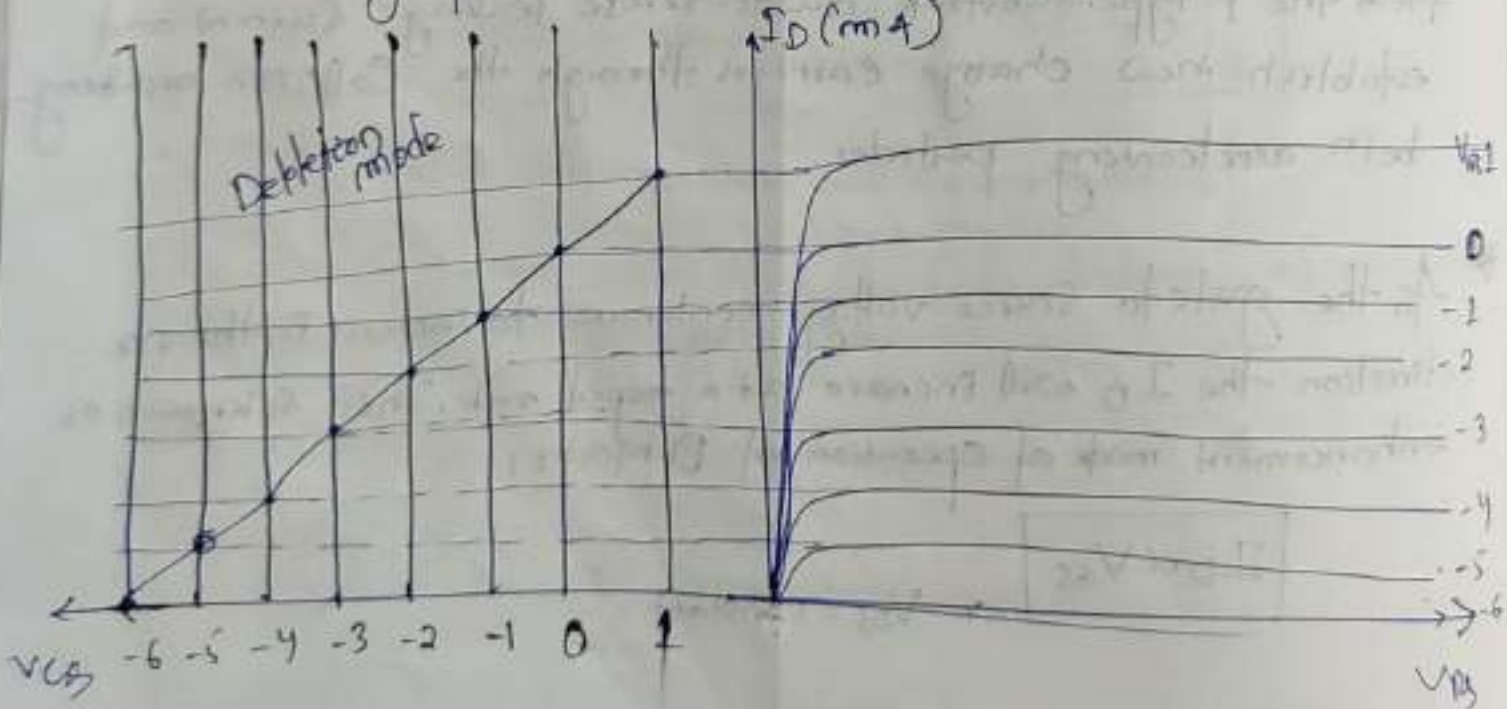


I_D, V_{GS} & V_{DS} for various value.

$V_{GS}=0$, $I_D=I_{DSS}$ (Maxm Saturation Current)

② Transfer characteristics of N channel DMOSFET:

It is the graph betn I_D Vs. V_{GS} for fixed V_{DS}.



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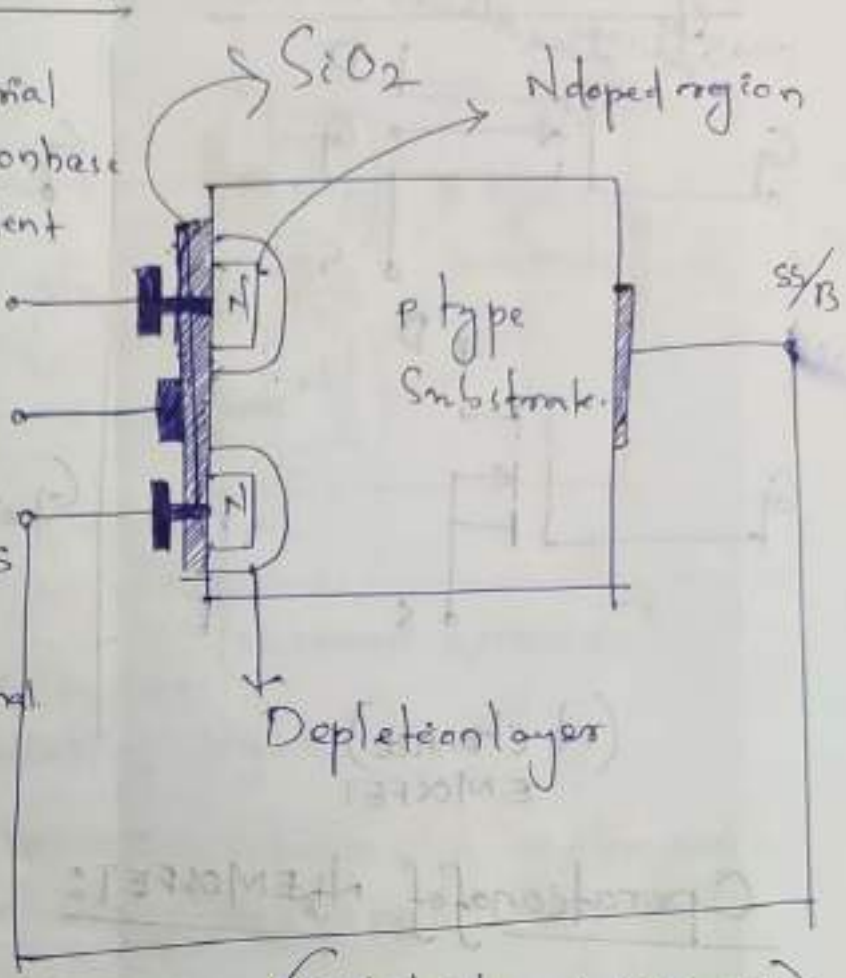
Construction of EMOSFET:

The slab of P-type material is formed from a silicon base then we will add trivalent impurity then we will have P-type substrate.



The substrate or base sometimes internally connected to source terminal OR used for external control of potential at source terminal.

(Fig. N-channel EMOSFET)

The source and drain terminals are connected through metallic contact to N-doped region.

This is the primary difference bet^n the construction of depletion MOSFET and E-MOSFET.

The gate is connected to the P-doped Substrate or P-substrate where via insulating layer of SiO_2.

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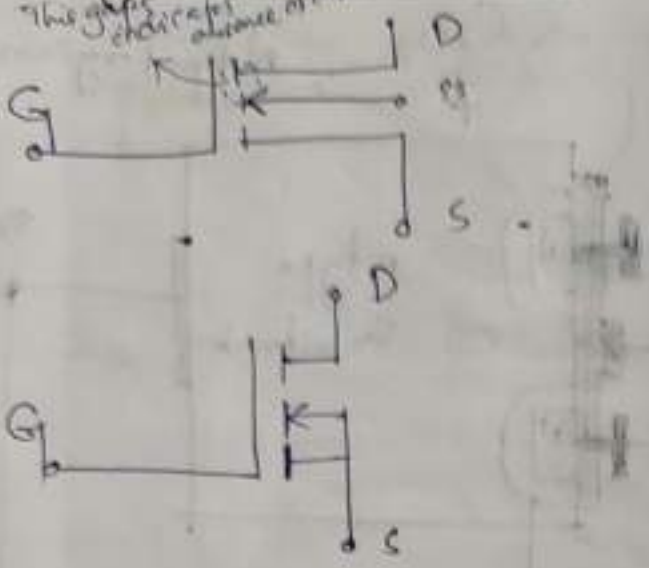
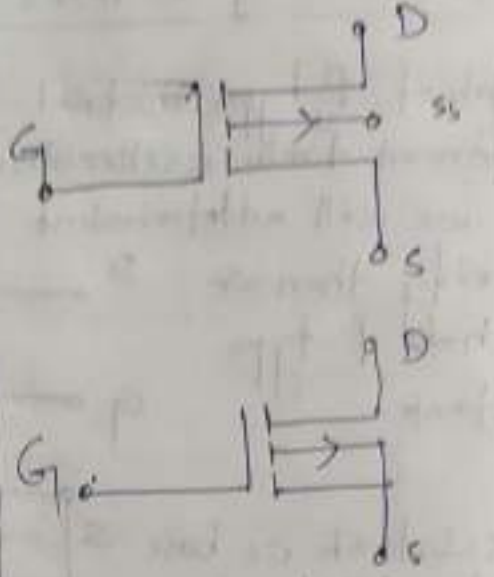
Symbole of EMOSFET:



(N-channel) EMOSFET



(P-channel) EMOSFET.

Operation of N-EMOSFET:

Case (i): When $V_{GS}=0$, $V_{DS}=+Ve$

If $V_{GS}=0$ and Voltage V_{DS} applied both drain and source of the device as shown in the fig. the absence of n-channel there is no current flow in the drain to source. It is not an sufficient to have a large accumulation of charge carriers at the drain and the source due to N doped regions.

Case (ii): When $V_{GS}=+Ve$ and $V_{DS}=+Ve$

If Both V_{GS} and V_{DS} having come +ve voltage (greater than 0V) establish the drain and gate at +ve Potential w.r.t Source.

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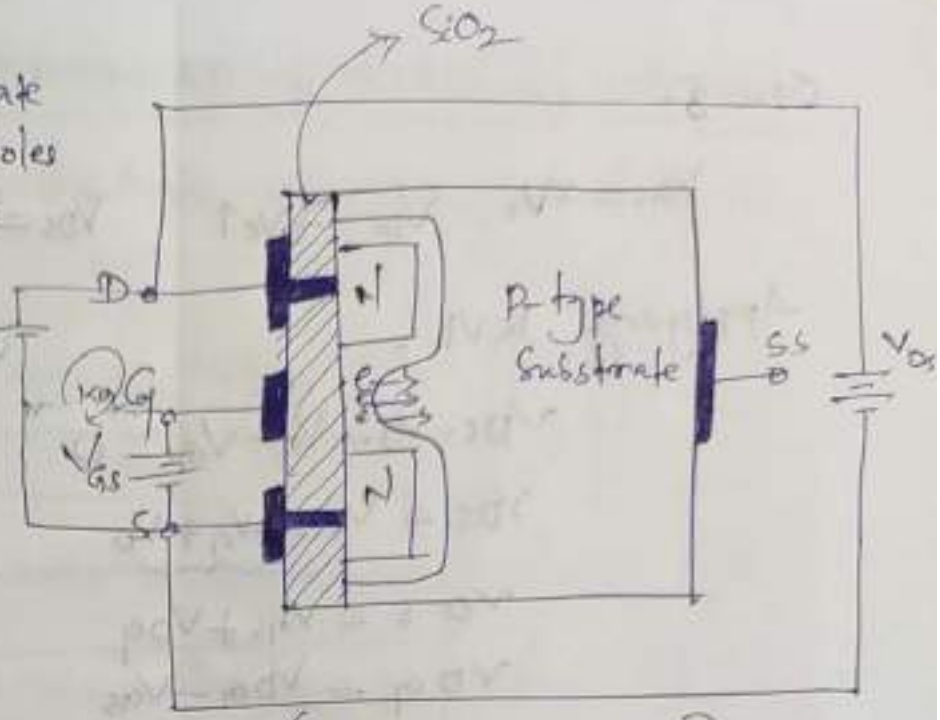
The +Ve Potential at gate will preserve the holes in the P-Substrate along N-doped Silicon dioxide (SiO_2) layer. To leave the area and enter deeper region of P-type substrate.



(N-channel EMOSFET)

The result in a depletion region nearer the SiO_2 insulating layer.

However the electrons in P-Substrate will be attracted to +Ve gate and accumulate in the region nearer the Surface of SiO_2 layer.

The SiO_2 layer and its insulating qualities will prevent the -Ve charge carriers from being observed at Gate terminal.

As V_{GS} increasing magnitude than concentration of electron nearer the SiO_2 Surface increases until eventually the induced n-type region can Support a majorable flow of Current bet^n drain to source.

The level of V_{GS} that in the significant increase in the drain Current is called Threshold voltage (V_T) since, channel is not existed with $V_{GS}=0V$ and enhanced by the application of +Ve gate to source voltage. This type of MOSFET is called enhancement MOSFET.

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Case 3:

V_{GS} = +Ve, V_{DS} = -ve ↑ $V_{DS} = |V_p|$, I_D = Constant

Applying KVL,

$$V_{DS} - V_D - V_G - V_{GS} = 0$$

$$V_{DS} = V_{GS} + V_G + V_D$$

$$V_{DS} = V_{GS} + V_{DG}$$

$$V_{DG} = V_{DG} - V_{GS}$$

$$= V_{DS} - V_T$$

$$\boxed{V_{DG} = V_{DS} - V_T}$$

* Saturation can be calculated by

$$\boxed{V_{DS}(Sat) = V_{GS} - V_T}$$

$V_{DS} = V_{DG} \Rightarrow I_D = I_S$ (At the

* To determine I_D at a given V_{GS}

$$\boxed{I_D = K(V_{GS} - V_T)^2}$$

K is the constant can be determined by using values of specific point and the formula

$$\boxed{K = \frac{I_D(ON)}{(V_{GS}(ON) - V_T)^2}}$$

where, V_T = Threshold voltage

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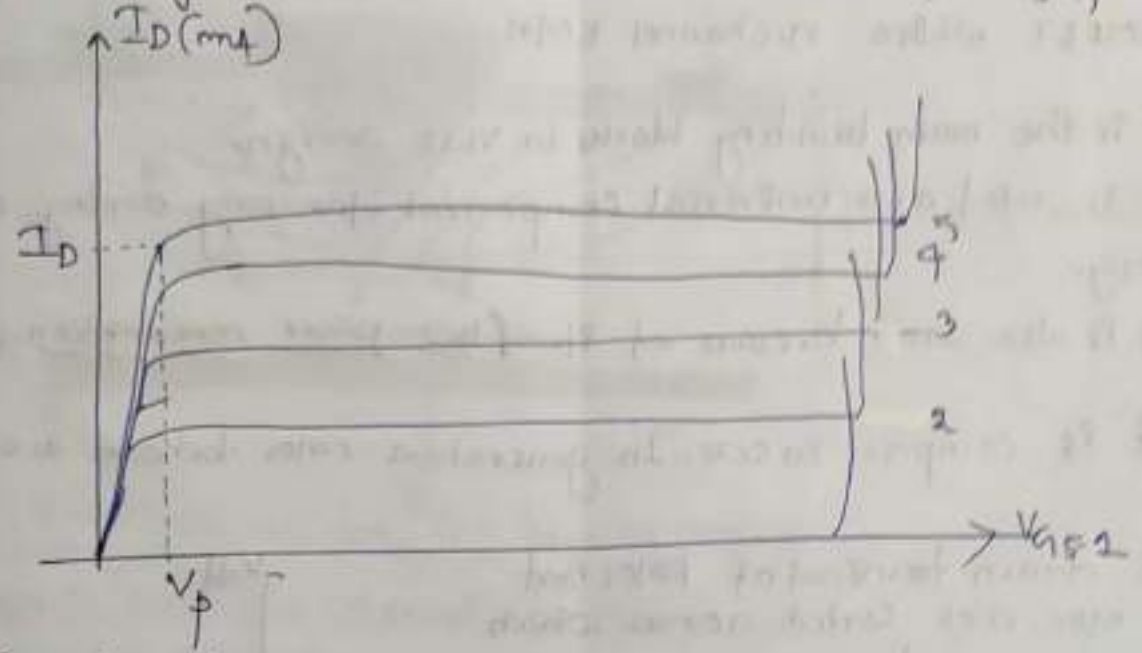
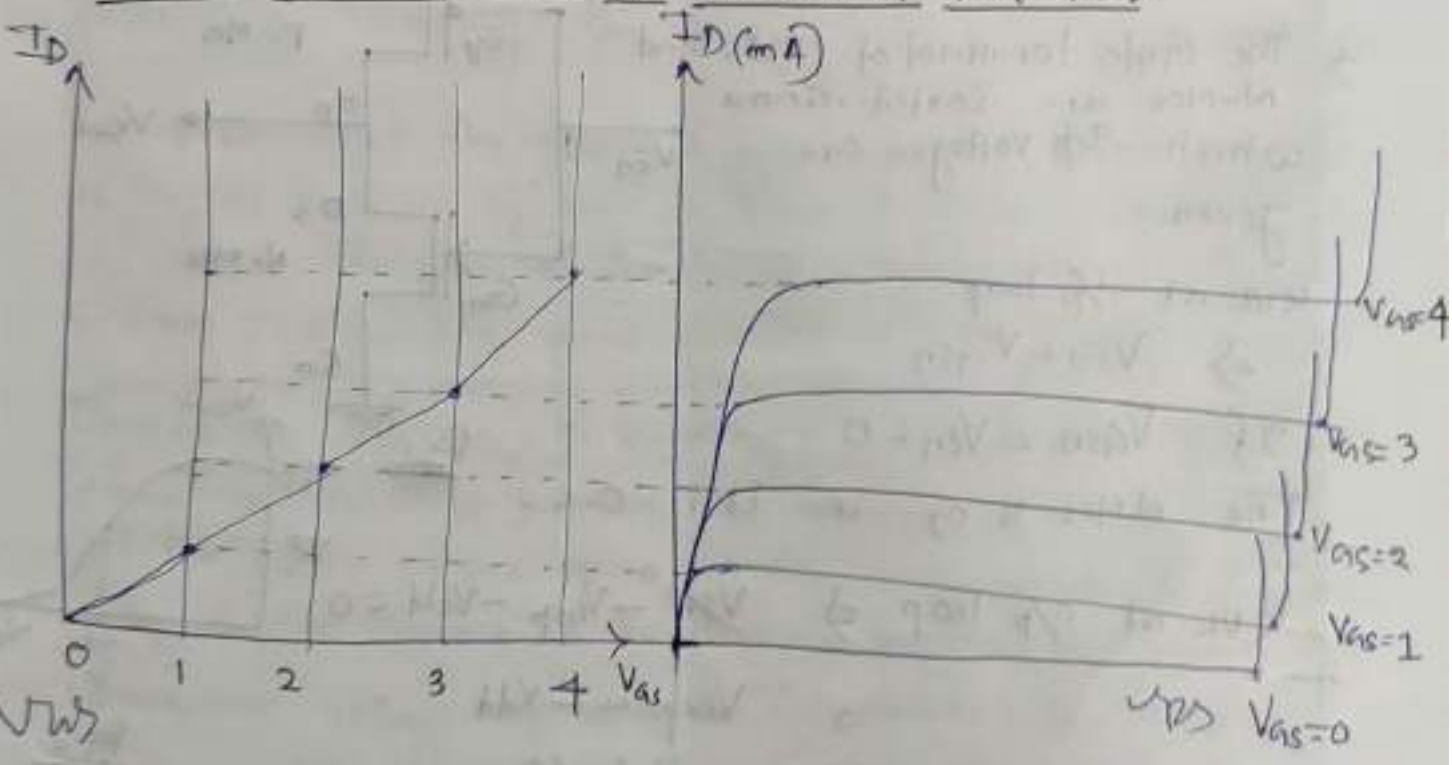
Output or Drain characteristics of N-channel EMOSFET:

* It is the graph bet^n I_D & V_{DS} at various values of V_{GS}.



Transfer characteristics of N-channel EMOSFET:



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Assignment

CMOS (Complementary MOSFET)

CMOS is a combination of a p-channel enhancement type MOSFET with a n-channel EMOS.

It is the main building blocks in VLSI design.
It is used as a universal component for any analog or digital design.
It is also used because of its low power consumption.

It is compact in size. In general a CMOS behaves as a inverter.

→ The drain terminal of PMOS and N-MOS are sorted across which output are taken.

→ The Gate terminal of PMOS and N-MOS are sorted across which i/p voltages are given.

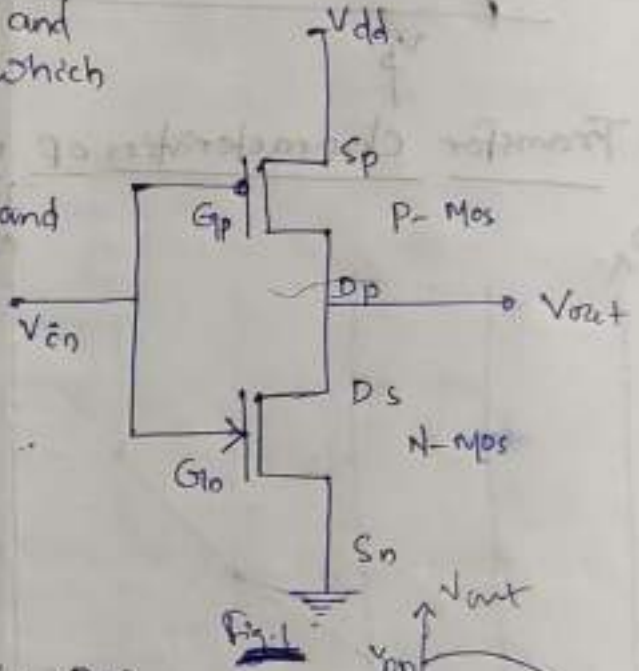

Fig-1

KVL at i/p loop

$\Rightarrow V_{in} = V_{GSn}$

If $V_{GSn} = V_{in} = 0$

The NMOS is off. i.e. it is O.C.

KVL at o/p loop $\Rightarrow V_{in}^{0} - V_{GSp} - V_{dd} = 0$

$\Rightarrow V_{GSp} = -V_{dd}$

So PMOS is on or it is SC.

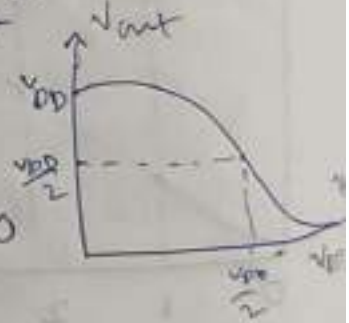

Fig-2

Since N-MOS is off and P-MOS is on the output voltage is equal to V_{dd}.

If V_{in} = high, then N-MOS will on & P-MOS will off the output will directly grounded, $V_o = 0V$.

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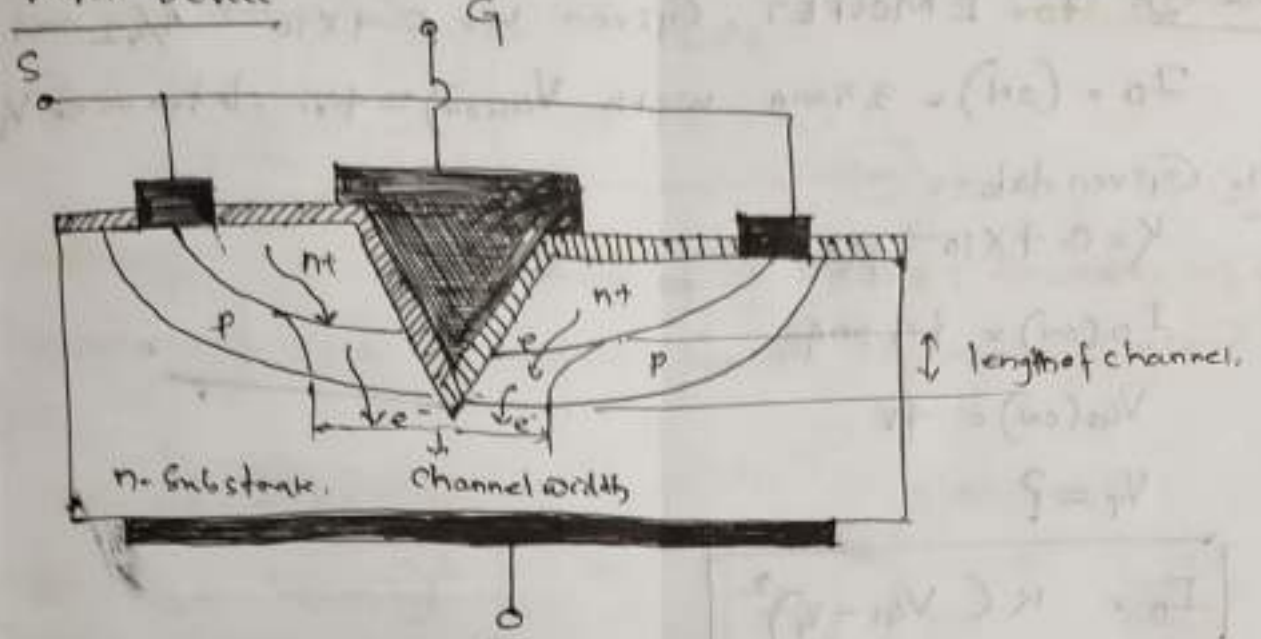
VMOS Device



A VMOS transistor is a type of MOSFET.

- VMOS is used for describing the V-groove shape vertically cut into the substrate material.

VMOS is an acronym for "Vertical metal oxide semiconductor"

The V shapes of the MOSFET's gate allows the device to deliver a higher amount of current from the source to the drain of the device. The shape of the depletion region creats a wider channel, allowing more current to flow through it.

During the operation in blocking mode, the highest electric field occurs at the n+/p+ junction. The presence of sharp corner at the bottom of the groove enhances the electric field at the edge of the channel in the depletion region, thus reducing breakdown voltage of the device. This electric field launches electrons into the gate oxide and consequently, the trapped electrons shift the threshold voltage of the MOSFET. For this reason, the V-groove architecture is no longer used in commercial device.

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Problem ①: For EMOSFET, Given $K = 0.4 \times 10^{-3}\ A/V^2$ and $I_{D(ON)} = 3.5mA$ with $V_{GS(ON)} = 4V$. determene V_T.

Soln: Given data:

$K = 0.4 \times 10^{-3}\ A/V^2$

$I_{D(ON)} = 3.5\ mA$

$V_{GS(ON)} = 4V$

$V_T = ?$

$$\boxed{I_D = K(V_{GS} - V_T)^2}$$

$$\Rightarrow 3.5mA = 0.4 \times 10^{-3} \frac{A}{V^2} (4V - V_T)^2$$

$$\Rightarrow \frac{3.5mA}{0.4 \times 10^{-3} A/V^2} = (4V - V_T)^2$$

$$\Rightarrow 8.75V = (4V - V_T)^2$$

$$\Rightarrow 2.95V = 4V - V_T$$

$$\Rightarrow \boxed{V_T = 1.05V} \quad \text{Ans}$$

Problem ② For a D MOSFET. Given $I_D = 4mA$ at $V_{GS} = 2$
Determene the saturation current. if $V_p = -4V$.

Ans: Given data. $I_D = 4mA$

$V_{GS} = -2V$

$V_p = -4V$

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$\Rightarrow I_{DSS} = \frac{I_D}{\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$

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$$I_{DSS} = \frac{4mA}{\left[1-\left(\frac{-2}{-4}\right)\right]^2} = 16mA$$

$$\therefore \boxed{I_{DSS} = 16mA} \quad \text{(Ans)}$$

Problem (8): Does the current of E-MOSFET increases of the same rate as a D-MOSFET for the conduction region?

Ans:

EMOSFET

$$\boxed{I_D = k(V_{GS} - V_T)^2}$$

const. → k and V_T

differentiating w.r.t V_{GS}

$$\frac{dI_D}{dV_{GS}} = k\frac{d}{dV_{GS}}(V_{GS}-V_T)^2$$

$$= 2kt\frac{dt}{dV_{GS}}$$

$$= 2k(V_{GS}-V_T)\frac{d(V_{GS}-V_T)}{dV_{GS}}$$

$$\boxed{\frac{dI_D}{dV_{GS}} = 2k(V_{GS}-V_T)}$$

$$= c(V_{GS}-c)$$

DMOSFET

$$\boxed{I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2}$$

const. → I_{DSS} and V_P

differentiating w.r.t V_{GS}.

$$\frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\cdot 2s\frac{ds}{dV_{GS}}$$

$$= I_{DSS}\cdot 2\left(1-\frac{V_{GS}}{V_P}\right)\left(0-\frac{1}{V_P}\right)$$

$$\boxed{\frac{dI_D}{dV_{GS}} = \frac{2I_{DSS}}{V_P^2}(V_{GS}-V_T)}$$

$\frac{2I_{DSS}}{V_P^2} = c$, $V_T = c$

$$= c(V_{GS}-c)$$

Hence from the above two expression we observed that,

Current of EMOSFET increases of the same rate as a DMOSFET.

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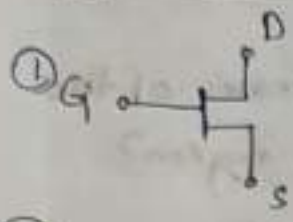
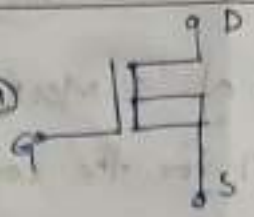
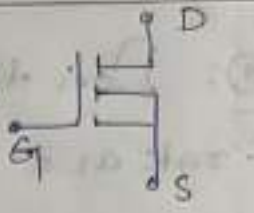
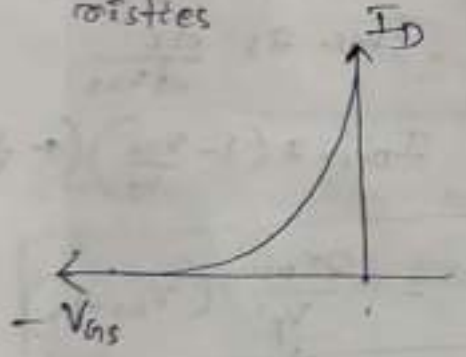
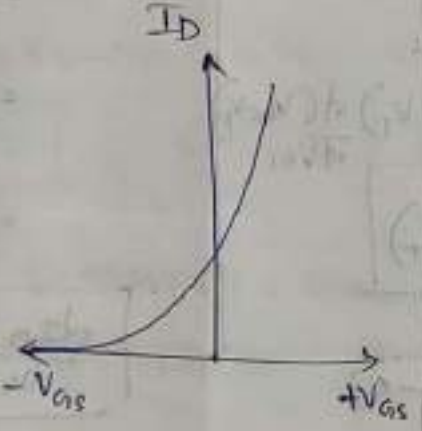
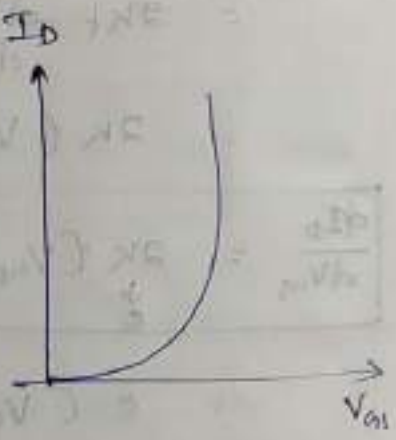
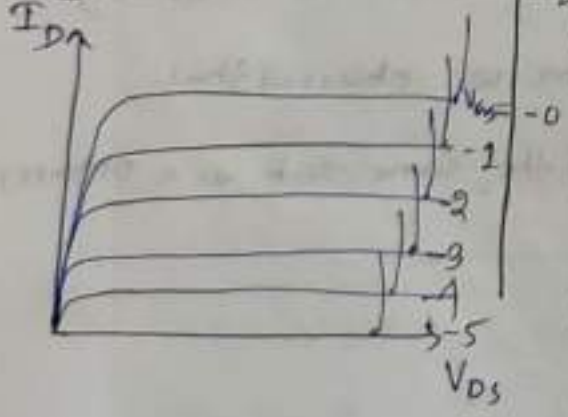
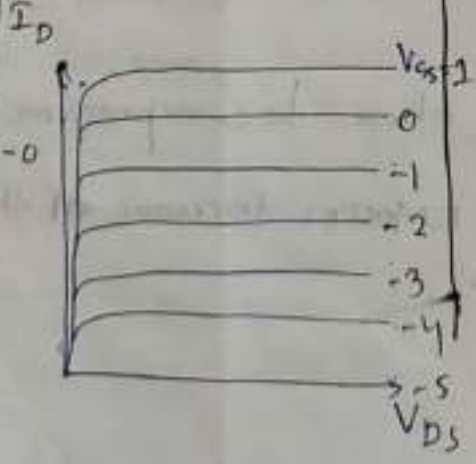
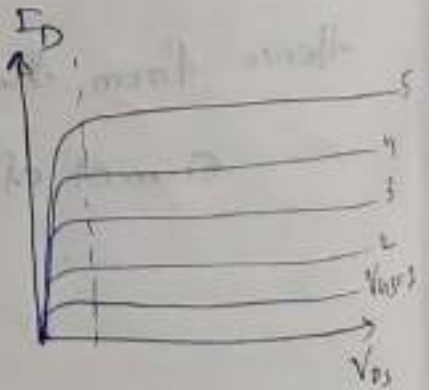
Summery:

JFET	DMOSFET	EMOSFET
① 	① 	① 
② $I_G=0,\ V_{GS}=0,\ I_D=I_S$	② $I_G=0,\ V_{GS}=0,\ I_D=I_S$	③ $I_G=0,\ V_{GS}=0,\ I_D=0$
*** ③ $I_D=I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$	*** $I_D=I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$	$I_D=K\left(V_{GS}-V_T\right)^2$
④ Transfer characteristics 		
⑤ Drain Current 		

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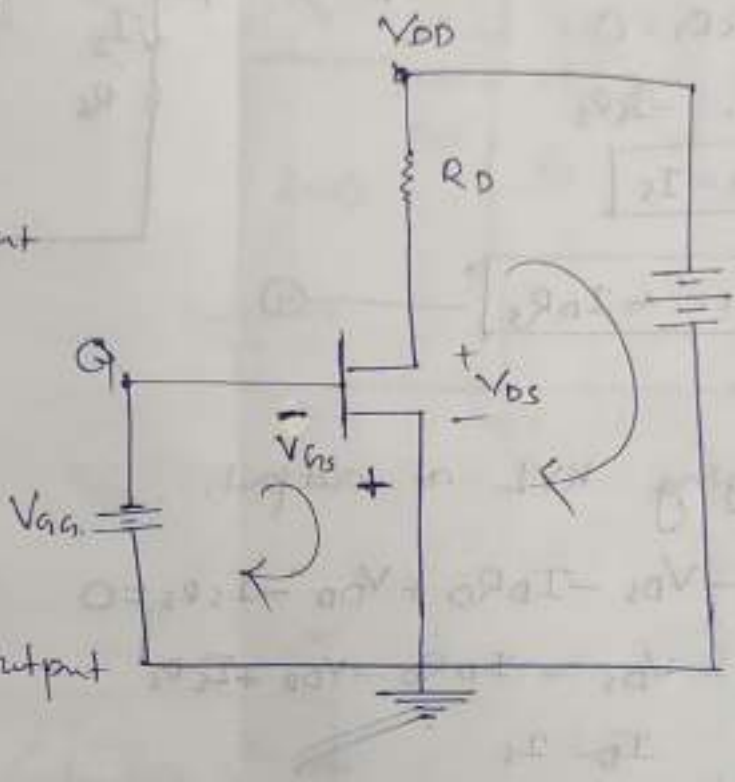
—: FET BIASING :—

1. fixed Bias of JFET
2. Self Bias of JFET
3. Voltage devider of JFET.

Fixed Bias JFET:



Applying KVL at input

$V_{GG} + V_{GS} = 0$

$$V_{GS} = -V_{GG}$$

Applying KVL at output side.

$$-V_{DS} - I_D R_D + V_{DD} = 0$$

$$-V_{DS} = I_D R_D - V_{DD}$$

$$V_{DS} = V_{DD} - I_D R_D$$

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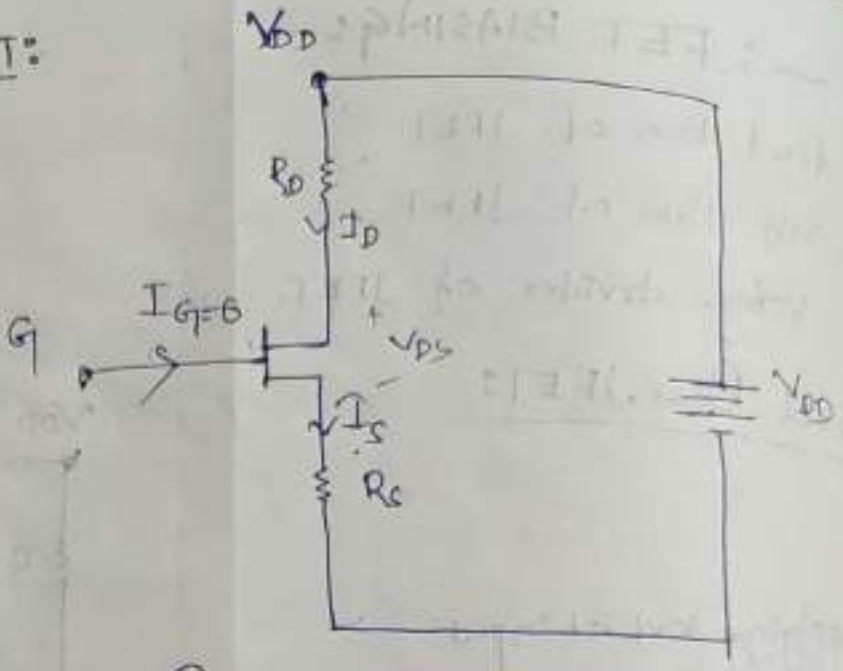
Self Bias of JFET:



KVL at input side,

$V_{GS} + I_S R_S = 0$

$V_{GS} = -I_S R_S$

$\boxed{I_D = I_S}$

$\boxed{V_{GS} = -I_D R_S}$ ——— (1)

Applying KVL at output,

$-V_{DS} - I_D R_D + V_{DD} - I_S R_S = 0$

$-V_{DS} = I_D R_D - V_{DD} + I_S R_S$

$I_D = I_S$

$-V_{DS} = I_D R_D - V_{DD} + I_D R_S$

$\boxed{V_{DS} = -I_D (R_D + R_S) + V_{DD}}$

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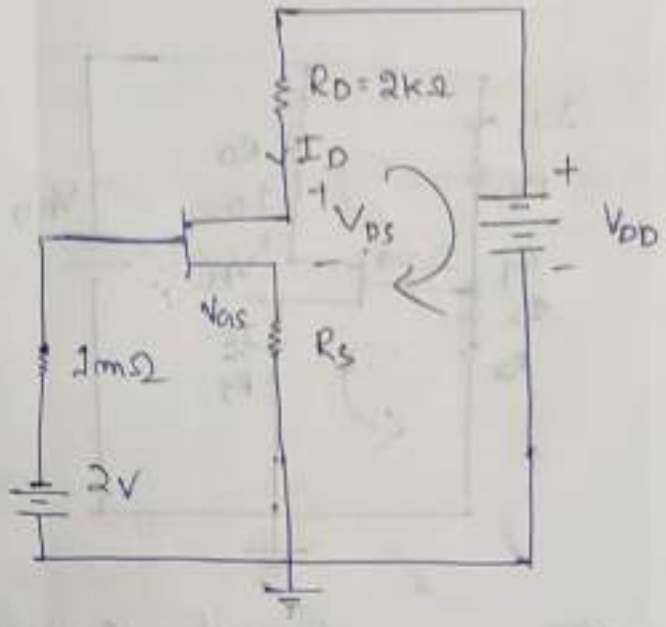
Problem: Determine the following for the network as shown in the fig.

Given data:

$I_{DSS} = 10mA$

$V_p = -8A$

V_S = ground



(a) V_{GS}

(b) I_D

(c) V_{DS}

(d) V_D

(e) V_G

Solution:

(a) $V_{GS} = -V_{GG}$

$= -2V$

(b) $\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2}$

$= 10mA\left(1 - \frac{1}{4}\right)^2 = 5625mA$

(c) $V_{DS} = V_{DD} - I_D R_D$

$= 16 - 5.625mA(2k\Omega)$

$= 4.75$

(d) $V_{DS} = V_D - V_S$

$V_D = V_{DS} + V_S$

$= 4.75 + 0V$

$= 4.75V$

(e) $V_{GS} = V_G - V_S$

$V_G = V_{GS} + V_S = -2 + 0 = -2V$

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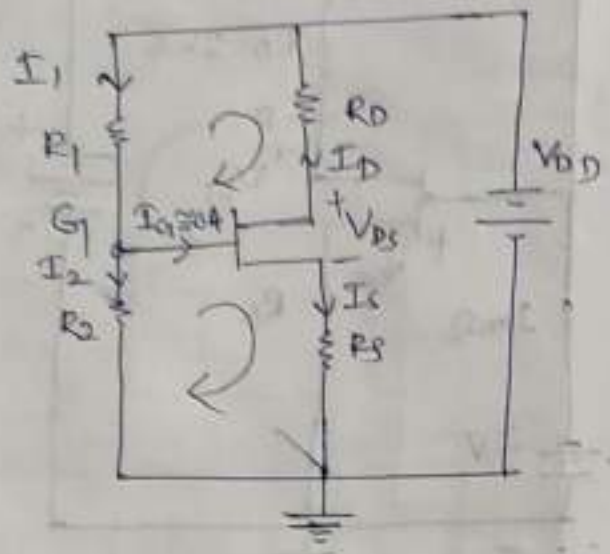
Voltage devider Beacing of JFET:



There is no flow of current in Gate terminal

So, $\boxed{I_1 = I_2}$ $\quad R = R_1 + R_2$

$V_G = I_2 R_2$ $\quad I = \frac{\text{Voltage}}{\text{Req}} = \frac{V_{DD}}{R_1+R_2}$

$$\boxed{V_G = \left(\frac{R_2}{R_1+R_2}\right) V_{DD}}$$ (Voltage drop across R_2)

Applying KVL i/p

$$-I_2 R_2 + V_{GS} + I_S R_S = 0$$

$$-V_G + V_{GS} + I_S R_S = 0$$

$$\boxed{V_G = V_{GS} + I_S R_S}$$

$V_{GS} = V_G - I_S R_S$

$$\boxed{V_{GS} = V_G - I_D R_S} \quad (\because I_D = I_S)$$

Applying KVL in output

$$-V_{DD} + I_S R_S + V_{DS} + I_D R_D = 0$$

$$\boxed{V_{DS} = I_D(R_S + R_D) + V_{DD}}$$

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Biasing of D MOSFET:

1. Self Bias
2. Voltage divider Bias

* D type MOSFET Bias ckt are similar to JFET Biasing ckt

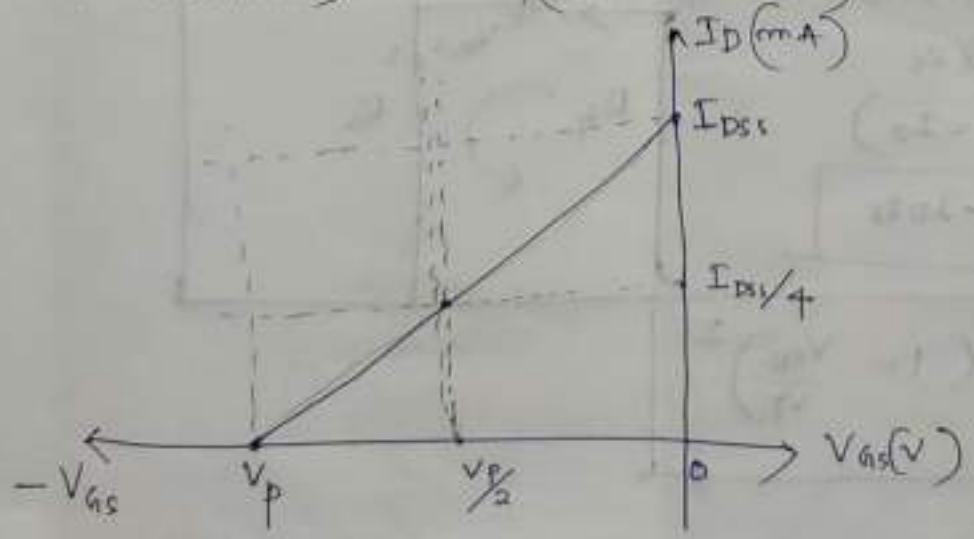
The only difference is that depletion type MOSFET can operate +Ve value of V_{GS} and with I_D values exceeds.

Q. Point = (V_{GSQ}, I_{DQ})

(1) Transfer characteristics:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

JFET (n-ch)	D MOSFET (n-ch)
$V_{GS} < 0V$	$V_{GS} < 0V$
$V_{GS} = 0V$	$V_{GS} = 0V$
$V_{GS} > 0V$ ✗	$V_{GS} > 0V$ ✓
I_{DD} (max)	I_{DD} is not max^m drain current
Q-pt - (-ve) or Zero (x-co-ordinate)	Q-pt → -ve or zero or +ve. (x-co-ordinate)



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Self Bias of DMOSFET:

Step 1: $V_{GS} = V_G$. $I_D = 0$

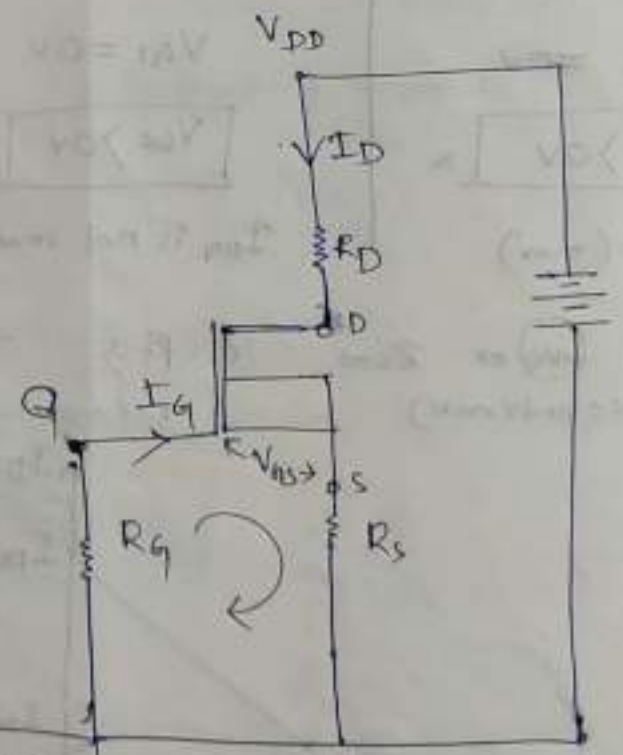
$I_D = V_G / R_S$, $V_{GS} = 0$

Step 2: Plot the transfer characteristics curve using I_{DSS}, V_P and Calculate values of I_D.

Step 3: The Q-point is located where the line intersects the transfer characteristics curve use the I_D at the Q-point to solve for the other variables, in the voltage divider Bias.

Understanding Purpose only

NOTE: Repeat all the steps of Self Biasing of JFET for DMOSFET Biasing.



KVL in i/p:

$I_G = 0$ & $R_G = 0$

KVL at input,

$V_G + I_S R_S = 0$

$V_{GS} + I_S R_S = 0$

$V_{GS} = -I_S R_S$.

$(\because I_S = I_D)$

$$V_{GS} = -I_D R_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

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Apply KVL at

$$V_{DD} - I_S R_S - V_{DS} - I_D R_D = 0$$

$$V_{DS} = V_{DD} - I_S R_S - I_D R_D$$

$\because I_S = I_D$

$$V_{DS} = V_{DD} - I_S R_S - I_D R_D$$

$$\boxed{V_{DS} = V_{DD} - I_D (R_S + R_D)}$$

2. Voltage divider Bias of DMOSFET:

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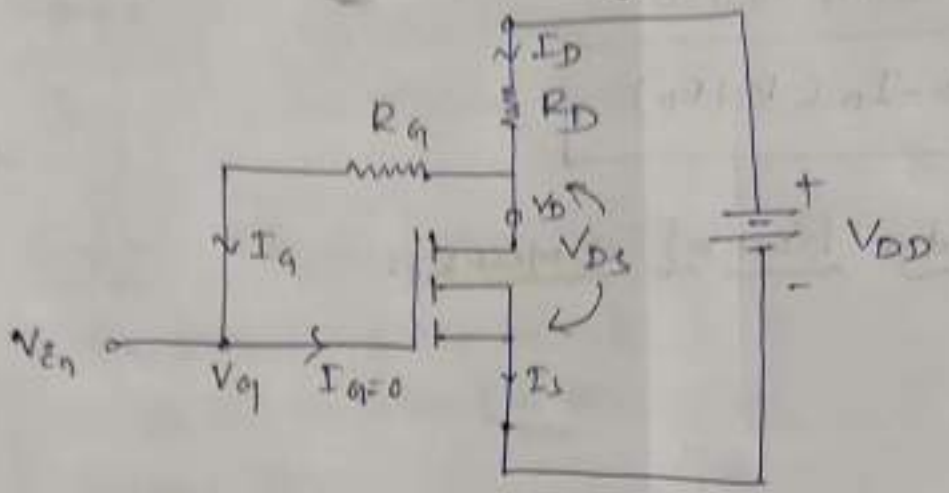
Biasing of EMOSFET:

1. Drain feedback Biasing
2. Voltage devide Biasing.

1. Drain feedback Biasing:



$$V_D - V_G = 0$$

$$V_D = V_G$$

$$\boxed{V_{DS} = V_{GS}}$$

Applying KVL at output side.

$$V_{DS} + I_D R_D - V_{DD} = 0$$

$$-V_{DS} - I_D R_D + V_{DD} = 0$$

$$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

$$\boxed{I_D = K(V_{GS} - V_T)^2}$$

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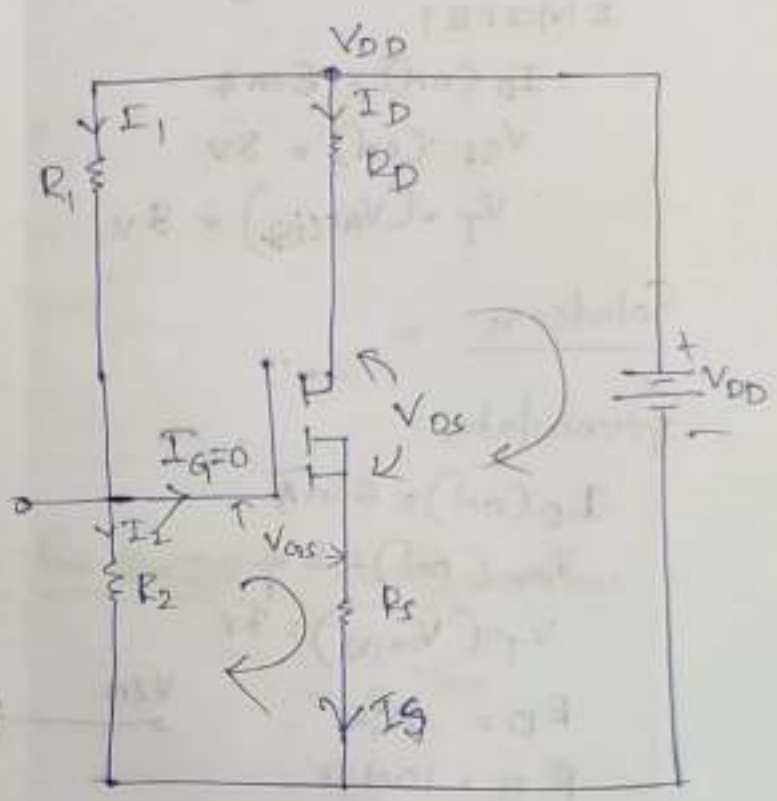
Voltage devider Bias of EMOSFET:



When $I_G = 0$,

$I_1 = I_2$

$V_G = I_2 R_2$

$= \frac{V_{DD}}{R_1+R_2} \times R_2$

Apply KVL at i/p side.

$-V_G + V_{GS} + I_S R_S = 0$

$V_{GS} = V_G - I_S R_S$

$= V_G - I_D R_S \quad (\because I_S = I_D)$

BJT	FET
I_C , V_{CE}	I_D, V_{DS} Buten EMOSFET voltage devider Biasing V_{GS}.

Apply KVL at output side.

$-I_S R_S - V_{DS} + V_{DD} - I_D R_D = 0$

$V_{DS} = V_{DD} - I_S R_S - I_D R_D$

$V_{DS} = V_{DD} - I_D(R_S + R_D) \quad (\because I_S = I_D)$

$\therefore \boxed{I_D = K(V_{GS} - V_T)^2}$

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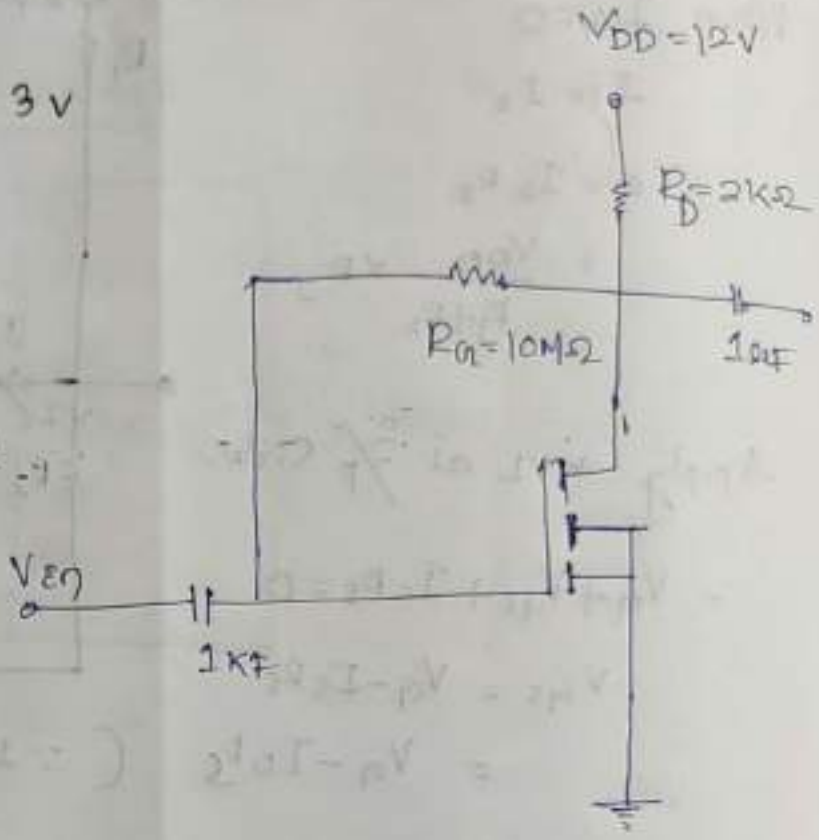
Problem: For the given N/w. find I_{DQ}, V_{DSQ} for the EMOSFET.

$I_{D(ON)} = 6mA$

$V_{GS(ON)} = 8V$

$V_T = (V_{GS(TH)}) = 3V$



Solution:

Given data:

$I_{D(ON)} = 6mA$

$V_{GS(ON)} = 8V$

$V_T = (V_{GS(TH)}) = 3V$

$R_D = 2K\Omega$

$R_G = 10M\Omega$

$V_{DD} = 12V$

$C_1 = 1KF$

$C_2 = 1uF$

$$I_D = K(V_{GS} - V_T)^2$$

$$K = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2} = \frac{6\times10^{-3}A}{(8-3)^2}$$

$$= \frac{6\times10^{-3}A}{5^2} = 0.24\times10^{-3}\ A/V^2$$

V_{GS} value between V_T & V_{GS} (3-8)V

$\therefore V_{GS} = 6V$

$I_{D1} = 0.24\ mA/V^2\ (6-3)^2$

$= 0.24 \times 9\ mA$

$= 2.16\ mA$

$V_{DS} = V_{DD} - I_D R_D$

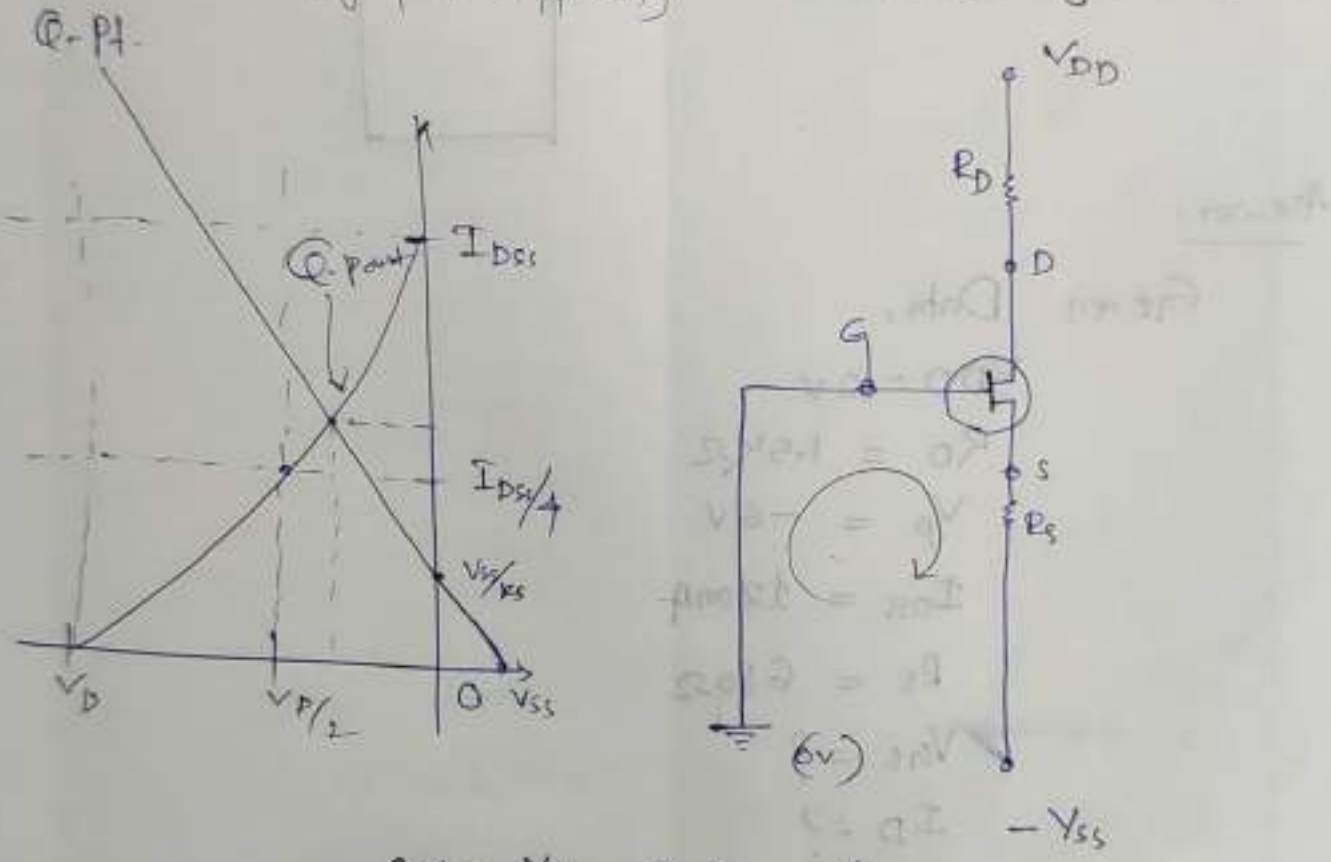
$= 12V - (2.16mA)(2k\Omega)$

$= 12 - 4.32$

$= 7.68\ V$

Common gate configuration for the JFET configuration:

(graphical Approach)



$0V - V_{GS} - I_D R_S = -V_{SS}$

$V_{GS} = V_{SS} - I_D R_S$ $\quad y = mx + c$

$I_D = \left(-\frac{1}{R_S}\right) V_{GS} + \boxed{\frac{V_{SS}}{R_S}}$ $\quad -c$

$V_{GS} = V_{SS}$

* Biasing is a operation to find the Q-point.

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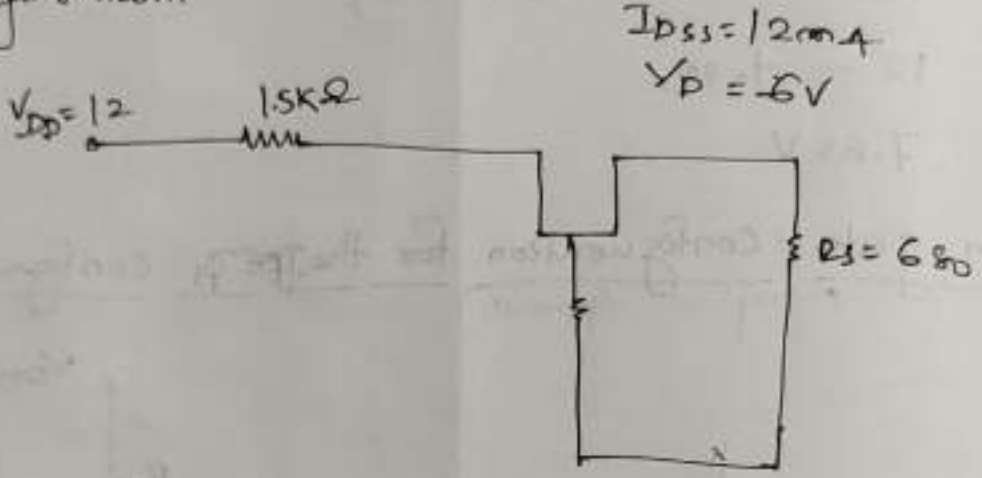
Applying KVL,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = -V_{SS}$$

$$V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$$

Problem: Determine the following for the common gate configuration.



Answer:

Given Data,

$V_{DD} = 12V$

$R_D = 1.5K\Omega$

$V_p = -6V$

$I_{DSS} = 12mA$

$R_S = 680\Omega$

$V_{GS} = ?$

$I_D = ?$

Here $V_{GS} = 0V$

$V_{GS} = 0 - I_D R_S$

$V_{GS} = -I_D R_S$

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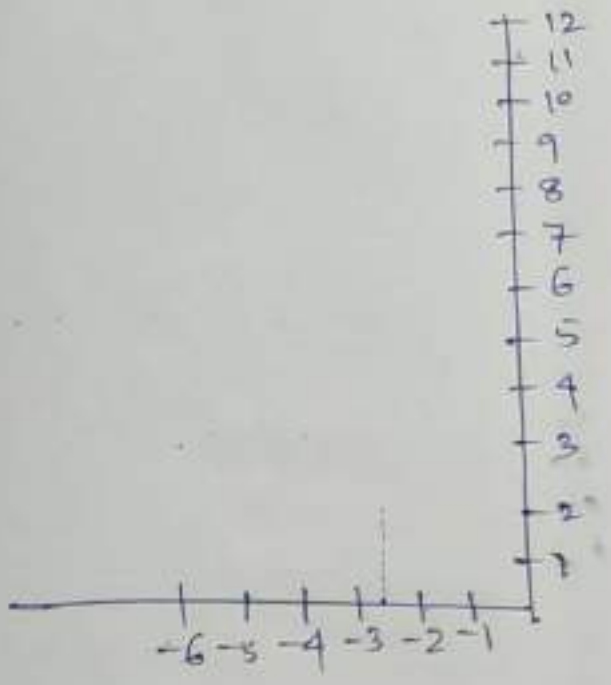

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