LECTURE NOTES

ON

ANALOG ELECTRONICS CIRCUIT

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Unit 1

Biasing of BJTs

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References: **1. "Principles of Electronics"**

VK Mehta

2. "Electronic Devices and Circuit Theory"

Robert L. Boylestad and L. Nashelsky

Bipolar Junction Transistor

Introduction

The transistor is a solid state device, whose operation depends upon the flow of electric charge carriers within the solid. Transistor is capable of amplification and in most respect it is analogous to a vacuum triode. The main difference between two is that the transistor is a current controlled device whereas vacuum triode is a voltage controlled device. The transistor is only about 6 decade old, yet it is replacing vacuum triode in almost all applications. The reasons are obviously its advantages over vacuum tubes such as

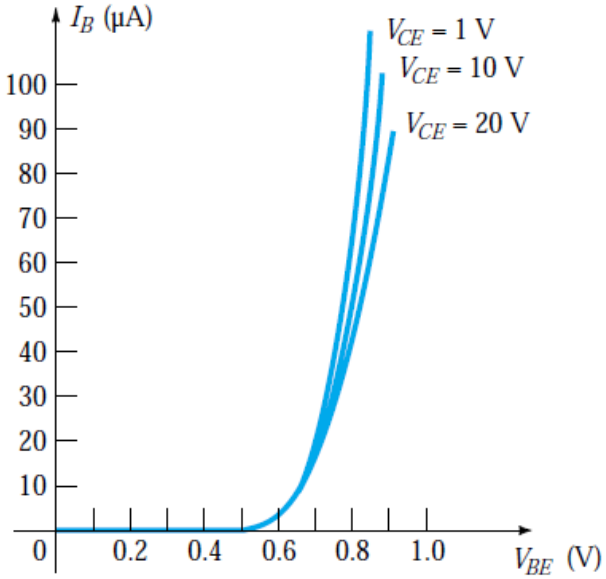
- ✓ Compact size
- ✓ Light weight
- ✓ Rugged construction
- ✓ More resistive to shocks and vibrations
- ✓ Instantaneous operation (no heating required)
- ✓ Low operating voltage
- ✓ High operating efficiency (no heat loss)
- ✓ Long life

However, transistors, in comparison to vacuum triodes, have some drawbacks also such as loud hum noise, restricted operating temperature (up to 75^0C) and operating frequency (up to a few MHz only).

Characteristics of CE transistor

Input characteristics

- ✓ The curve drawn between base current I_B and base-emitter voltage V_{BE} for a given value of collector-emitter voltage V_{CE} is known as the input characteristics.
- ✓ For determination of input characteristics, collector-emitter voltage V_{CE} is held constant and base current I_B is recorded for different values of base-emitter voltage V_{BE}.
- ✓ Now the curves are drawn between base current I_B and base-emitter voltage V_{BE} for different values of V_{CE}, as shown in figure



- ✓ The input characteristics of CE transistors are quiet similar to those of a forward biased diode because the bas-emitter region of the transistor is a diode and it is forward biased.

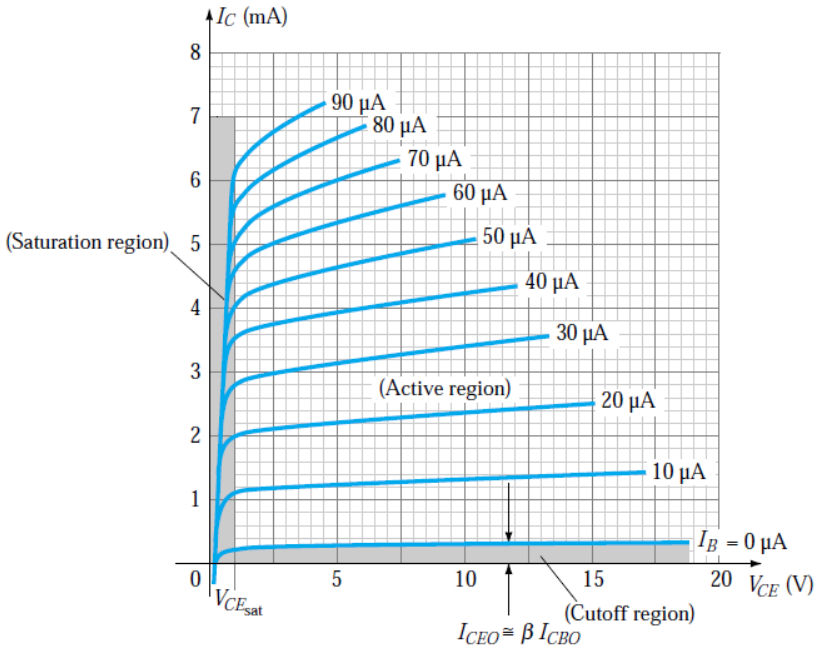
Output Characteristics

- ✓ Output characteristic of a common emitter transistor is the curve drawn between collector current I_C and collector-emitter voltage V_{CE} for a given value of base current I_B.

- ✓ For determination of common emitter output characteristics, base current I_B is maintained at several convenient levels.

- ✓ At each fixed level of I_B, collector-emitter voltage V_{CE} is adjusted in steps, and the corresponding values of collector current I_C are noted.

- ✓ Thus, a family of characteristics is obtained which are typically as illustrated in Figure



The points regarding output characteristics are given below

- ✓ The collector current I_C varies with V_{CE} for V_{CE} between 0 and 1V and then becomes almost constant and independent ofV_{CE}. The transistors are always operated above 1V.

- ✓ Output characteristic in CE configuration has some slope while CB configuration has almost horizontal characteristics.

- ✓ In active region (collector junction reverse biased and emitter junction forward biased), for small values of base current $I_B$the effect of collector voltage over I_C is small but for large values of $I_C$this effect increases.

- ✓ With low values (ideally zero) of $V_{CE}$the transistor is said to be operated in saturation region and in this region base current I_B does not cause a corresponding change in collector currentI_C.

- ✓ With much higher V_{CE}, the collector-base junction completely breakdown and because of this avalanche breakdown collector current I_C increases rapidly and the transistor gets damaged.

- ✓ In cut off region, small amount of collector current I_C flows even when base current $I_B = 0$. This is called I_{CEO}. Since main current I_C is zero, the transistor is said to be cut-off.

Faithful Amplification

The basic function of transistor is to do amplification.

The weak signal is given to the base of the transistor and amplified output is obtained in the collector circuit. One important requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. This increase in magnitude of the signal without any change in shape is known as *faithful amplification*.

In order to achieve this, means are provided to ensure that input circuit (*i.e.* base-emitter junction) of the transistor remains forward biased and output circuit (*i.e.* collector base junction) always remains reverse biased during all parts of the signal. This is known as *transistor biasing*.

The process of raising the strength of a weak signal without any change in its general shape is known as faithful amplification.

The theory of transistor reveals that it will function properly if its input circuit (i.e. base-emitter junction) remains forward biased and output circuit (i.e. collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied.

(i) Proper zero signal collector current

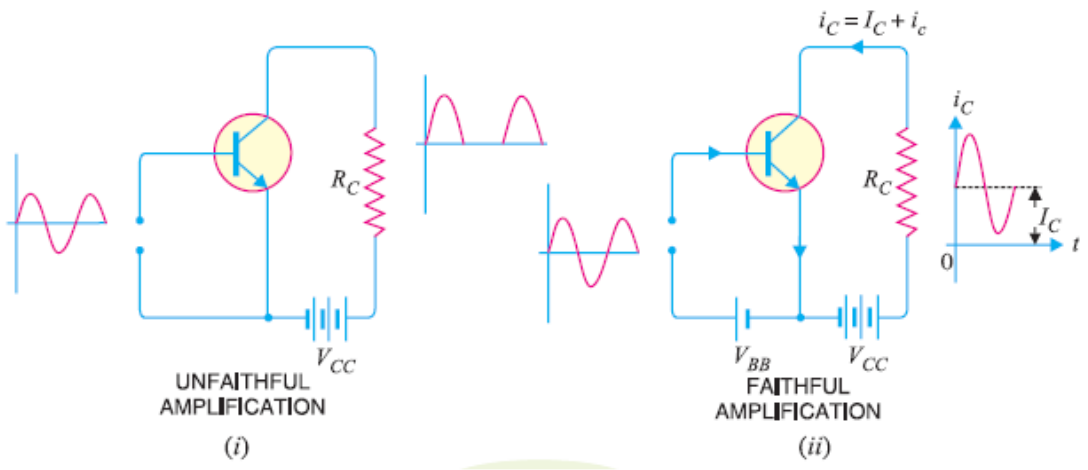
(ii) Minimum proper base-emitter voltage (V_{BE}) at any instant

(iii) Minimum proper collector-emitter voltage (V_{CE}) at any instant

The conditions (i) and (ii) ensure that base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, condition (iii) ensures that base-collector junction shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics i.e. between saturation to cut off.

Proper zero signal collector current

Consider an npn transistor circuit shown in Fig. During the positive half-cycle of the signal, base is positive w.r.t. emitter and hence base emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that positive half-cycle of the signal is amplified in the collector as shown. However, during the negative half-cycle of the signal, base-emitter junction is reverse biased and hence no current flows in the circuit. The result is that there is no output due to the negative half cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is unfaithful amplification.



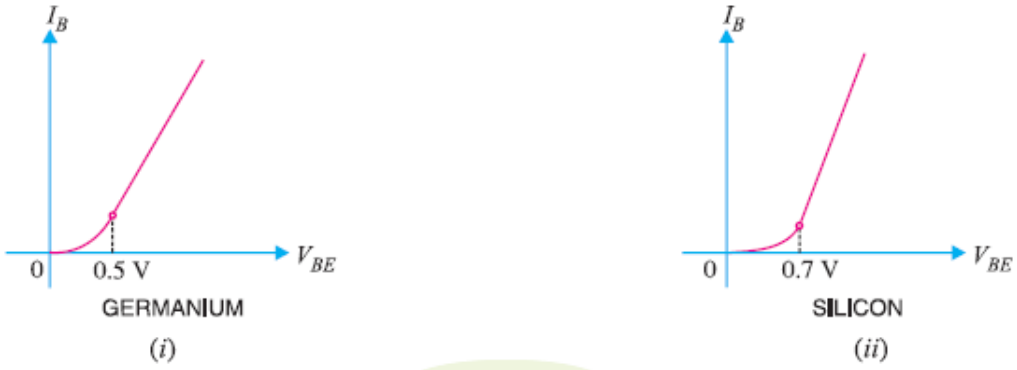
Now, introduce a battery source V_{BB} in the base circuit as shown in Fig. The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} as shown. This is known as zero signal collector current I_C. During

the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases. However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases. In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows, therefore, that for faithful amplification, proper zero signal collector current must flow. The value of zero signal collector current should be at least equal to the maximum collector current due to signal alone i.e.

Zero signal collector current $\geq$ Maximum collector current due to signal alone

Proper minimum base-emitter voltage.

In order to achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below 0.5V for germanium transistors and 0.7V for Si transistors at any instant.

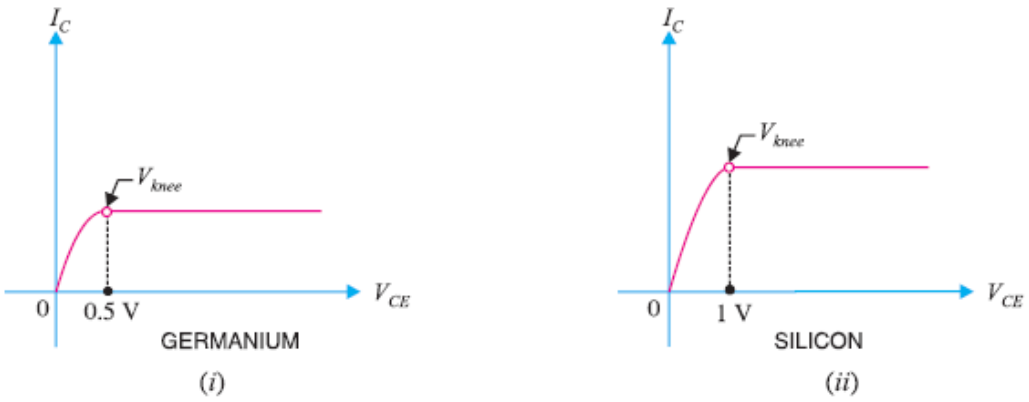


The base current is very small until the input voltage overcomes the potential barrier at the base-emitter junction. The value of this potential barrier is 0.5V for Ge transistors and 0.7V for Si transistors as shown in Fig. Once the potential barrier is overcome, the base current and hence collector current increases sharply. Therefore, if base-emitter voltage V_{BE} falls below these values during any part of the signal, that part will be amplified to lesser extent due to small collector current.

This will result in unfaithful amplification.

Proper minimum V_{CE} at any instant.

For faithful amplification, the collector-emitter voltage V_{CE} should not fall below 0.5V for Ge transistors and 1V for silicon transistors. This is called knee voltage (See Fig.).

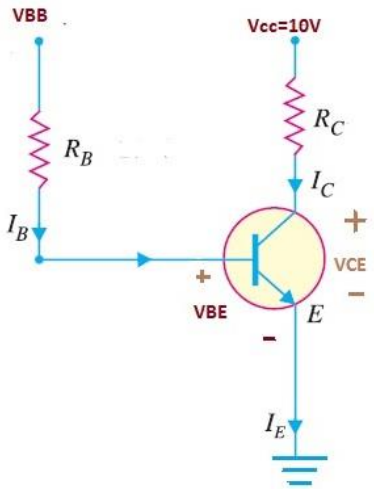


When V_{CE} is too low (less than 0.5V for Ge transistors and 1V for Si transistors), the collector base junction is not properly reverse biased. Therefore, the collector cannot attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base. This decreases the collector current while base current increases. Hence, value of β falls. Therefore, if V_{CE} is allowed to fall below V_{Knee} during any part of the signal, that part will be less amplified due to reduced β. This will result in unfaithful amplification. However, when V_{CE} is greater than V_{Knee}, the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

Numerical:

For the circuit shown in the Fig. has $R_B = 10\ K\Omega$ and$R_C = 1\ K\Omega$, it is required to determine the value of V_{BB} that results the transistor operating a) in the active mode with $V_{CE} = 5V$, b) at the edge of saturation c) deep in saturation with $\beta_{forced} = 10$

For simplicity, assume that$V_{BE} = 0.7V$. The transistor has $\beta = 50$



a) $I_C = \frac{V_{CC}-V_{CE}}{R_C} = \frac{10V-5V}{1K\Omega} = 5mA$

$$I_B = {}^{I_C}/_{\beta} = \frac{5mA}{50} = 0.1mA$$

$$V_{BB} = I_B R_B + V_{BE}$$
$$= 0.1 \times 10 + 0.7 = 1.7V$$

b) $\boldsymbol{V_{CE} = V_{CE_{sat}} \approx 0.3V}$

$$I_C = \frac{V_{CC}-V_{CE_{sat}}}{R_C} = \frac{10V-0.3V}{1K\Omega} = 9.7mA$$

$$I_B = {}^{I_C}/_{\beta} = \frac{9.7mA}{50} = 0.194mA$$

$$V_{BB} = I_B R_B + V_{BE}$$
$$= 0.194 \times 10 + 0.7 = 2.64V$$

c) $\boldsymbol{V_{CE} = V_{CE_{sat}} \approx 0.2V}$

$$I_C = \frac{V_{CC} - V_{CE_{sat}}}{R_C} = \frac{10V - 0.2V}{1K\Omega} = 9.8mA$$

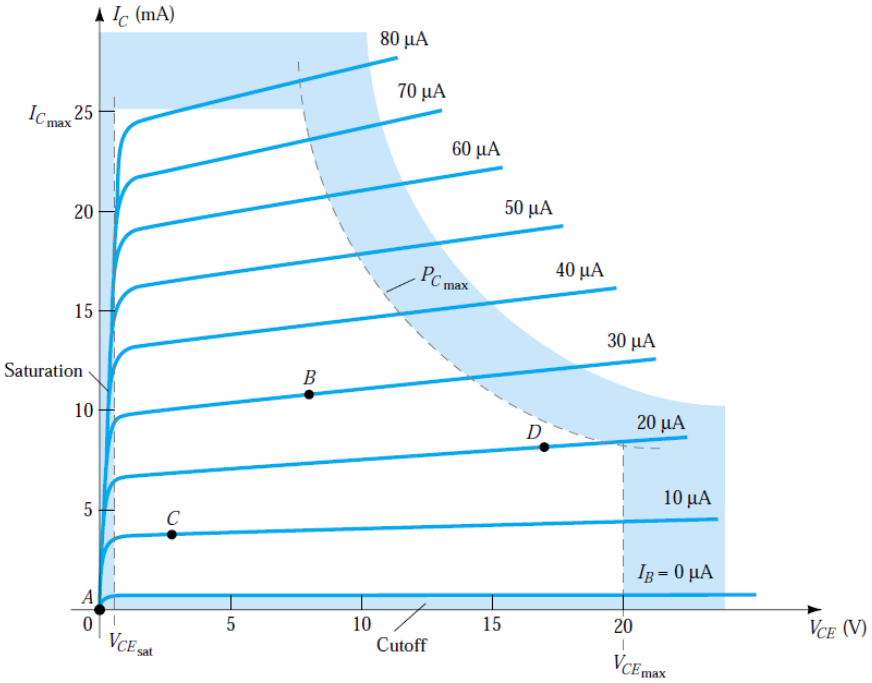
$$I_B = {I_C}/{\beta_{forced}} = \frac{9.8mA}{10} = 0.98mA$$

$$V_{BB} = I_B R_B + V_{BE}$$

$$= 0.98 \times 10 + 0.7 = 10.5V$$

OPERATING POINT

For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point). By definition, quiescent means quiet, still, inactive. Figure shows a general output device characteristic with four operating points indicated.



Point A

If no bias were used, the device would initially be completely off, resulting in a *Q*-point at *A*-namely, zero current through the device (and zero voltage across it). Since it is necessary to bias a device so that it can respond to the entire range of an input signal therefore point *A* would not be suitable.

Point C

At point C near cut-off region, the output currentI_C and output voltage V_{CE} would be allowed to vary, but clipped at negative peaks for a sinusoidally varying signal. So it is not the suitable operating point.

Point B

In this case when the signal is applied to the circuit, collector voltage and current will vary approximately symmetrical around the quiescent values of I_C and V_{CE} and amplify both positive and negative parts of input signal. In this case the voltage and current of the device will vary, but not enough to drive the device into saturation or cut off region. Usually, the amplifier action occurs within the operating region of the device between cut-off and saturation. So at point B located at centre of the load line is the best operating point in terms of linear gain or largest possible voltage and current swing variation.

Bias Stabilisation

The collector current in a transistor changes rapidly when

- ✓ The temperature changes,
- ✓ The transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

When the temperature changes or the transistor is replaced, the operating point (*i.e.* zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. This necessitates to make the operating point independent of these variations. This is known as bias stabilisation.

The process of making operating point independent of temperature changes or variations in transistor parameters is known as bias **stabilisation.**

Once stabilisation is done, the zero signal I_C and V_{CE} become independent of temperature variations or replacement of transistor *i.e.* the operating point is fixed. A good biasing circuit always ensures the stabilisation of operating point.

Need for stabilisation

Stabilisation of the operating point is necessary due to the following reasons:

- ✓ Temperature dependence of I_C
- ✓ Individual variations
- ✓ Thermal runaway

Temperature dependence of I_C

The collector current I_C for CE circuit is given by:

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

The collector leakage current I_{CO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 10°C doubles the collector leakage current which may be as high

as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal I_C = 1mA, therefore, the change in I_C due to temperature variations cannot be tolerated. This necessitates to stabilise the operating point *i.e.* to hold I_C constant inspite of temperature variations.

Individual variations

The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates to stabilise the operating point i.e. to hold I_C constant irrespective of individual variations in transistor parameters.

Thermal runaway.

The collector current for a CE configuration is given by :

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

The collector leakage current I_{CO} is strongly dependent on temperature. The flow of collector current produces heat within the transistor. This raises the transistor temperature and if no stabilisation is done, the collector leakage current I_{CO} also increases. It is clear from exp. (i) that if I_{CO} increases, the collector current I_C increases by (β + 1) I_{CO}. The increased I_C will raise the temperature of the transistor, which in turn will cause I_{CO} to increase. This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out.

The self-destruction of an unstabilised transistor is known as **thermal runaway.**

In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is stabilised i.e. I_C is kept constant. In practice, this is done by causing I_B to decrease automatically with temperature increase by circuit modification. Then decrease in βI_B will compensate for the increase in $(\beta + 1) I_{CO}$, keeping Ic nearly constant. In fact, this is what is always aimed at while building and designing a biasing circuit.

Stability Factor

Stability Factor due to leakage current

It is desirable and necessary to keep I_C constant in the face of variations of I_{CO}. The extent to which a biasing circuit is successful in achieving this goal is measured by stability factor S. It is defined as under:

The rate of change of collector current I_C w.r.t. the collector leakage current I_{CO} at constant β and V_{BE} is called stability factor i.e.

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} \quad \text{Where } V_{BE} \text{ and } \beta \text{ are constant}$$

The stability factor indicates the change in collector current I_C due to the change in collector leakage current I_{CO}. Thus stability factor 50 of a circuit means that I_C changes 50 times as much as any change in I_{CO}. In order to achieve greater thermal stability, it is desirable to have as low stability factor as possible. The ideal value of S is 1 but it is never possible to achieve it in practice. Experience shows that values of S exceeding 25 result in unsatisfactory performance.

Stability Factor due to base-emitter voltage V_{BE}

The rate of change of collector current I_C w.r.t. base-emitter voltage at constant β and I_{CO} is called stability factor due to base-emitter voltage i.e.

$$S(V_{BE}) = \frac{dI_C}{dV_{BE}} \quad \text{Where } \beta \text{ and } I_{CO} \text{ are constant}$$

Stability Factor due to β

The rate of change of collector current I_C w.r.t. β at constant base-emitter voltage and I_{CO} is called stability factor due to current gain β i.e.

$$S(\beta) = \frac{dI_C}{d\beta} \quad \text{Where } V_{BE} \text{ and } I_{CO} \text{ are constant}$$

General expression for $S(I_{CO})$

In the active region, the basic relationship between I_C and I_B is given by

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

Differentiating both sides w.r.t I_C keeping β as constant

$$\frac{dI_C}{dI_C} = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

$$1 - \beta \frac{dI_B}{dI_C} = (\beta + 1) \frac{1}{S(I_{CO})}$$

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta \frac{dI_B}{dI_C}}$$

The value of $\frac{dI_B}{dI_C}$ depends upon the biasing arrangement used and for determination of the stability factor S (I_{CO}) it is only necessary to find the relationship between I_C and I_B.

General expression for S (β)

In the active region, the basic relationship between I_C and I_B is given by

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

Differentiating both sides w.r.t I_C keeping I_{CO} as constant

$$1 = \beta \frac{dI_B}{dI_C} + I_B \frac{d\beta}{dI_C} + I_{CO} \frac{d\beta}{dI_C}$$

$$\frac{d\beta}{dI_C}(I_B + I_{CO}) = 1 - \beta \frac{dI_B}{dI_C}$$

$$\frac{1}{S(\beta)}(I_B + I_{CO}) = 1 - \beta \frac{dI_B}{dI_C}$$

$$S(\beta) = \frac{I_{CO} + I_B}{1 - \beta \frac{dI_B}{dI_C}}$$

Transistor Biasing

It has already been discussed that for faithful amplification, a transistor amplifier must satisfy three basic conditions, namely: (i) proper zero signal collector current, (ii) proper base-emitter voltage at any instant and (iii) proper collector-emitter voltage at any instant. It is the fulfilment of these conditions which is known as transistor biasing.

The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as *transistor biasing*.

The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal. This can be achieved with a bias battery or associating a circuit with a transistor. The latter method is more efficient and is frequently employed. The circuit which provides transistor biasing is known as biasing circuit. It may be noted that transistor biasing is very essential for the proper operation of transistor in any circuit.

Methods of Transistor Biasing

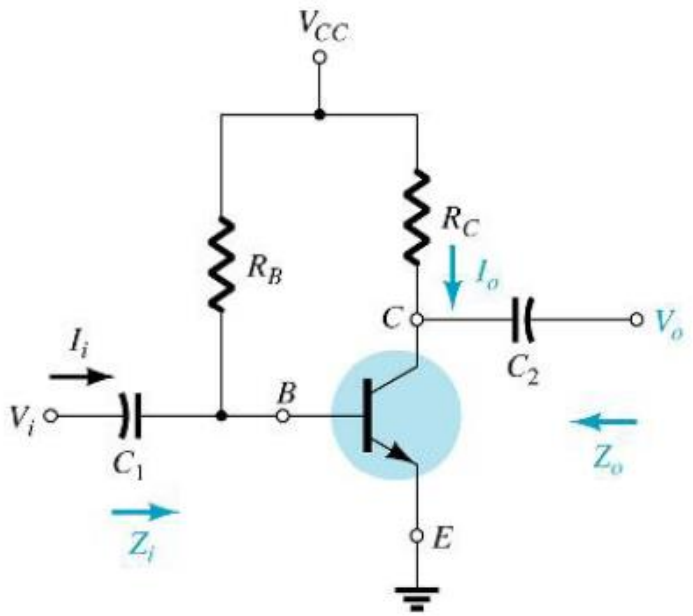
In the transistor amplifier circuits drawn so far biasing was done with the aid of a battery V_{BB} which was separate from battery V_{CC} used in the output circuit. However, in the interest of simplicity and economy it is desirable that transistor circuit should have a single source of supply—the one in the output circuit i.e V_{CC}). The following are the most commonly used methods of obtaining transistor biasing from one source of supply V_{CC}.

- ✓ Base resistor or fixed bias method
- ✓ Emitter bias method
- ✓ Biasing with collector-feedback resistor
- ✓ Voltage-divider bias

In all these methods, the same basic principle is employed i.e. required value of base current (and hence I_C) is obtained from V_{CC} in the zero signal conditions. The value of collector load R_C is elected keeping in view that V_{CE} should not fall below 0.5 V for germanium transistors and 1V for silicon transistor.

Fixed-Bias Circuit

In this method, a high resistance R_B (several hundred kΩ) is connected between the base and +ve end of supply for *npn* transistor (See Fig.) and between base and negative end of supply for *pnp* transistor. Here, the required zero signal base current is provided by V_{CC} and it flows through R_B. It is because now base is positive *w.r.t.* emitter *i.e.* base-emitter junction is forward biased. The required value of zero signal base current I_B (and hence $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor R_B.



Input loop

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Since V_{BE} is small as compared to V_{CC}

$$I_B \cong \frac{V_{CC}}{R_B}$$

Output loop

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

Stability Factors in Fixed-bias Circuit

S (I_{CO}):-

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} \quad Where\ V_{BE}\ and\ \beta\ are\ constant$$

General expression for S (I_{CO}) is given by

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta \frac{dI_B}{dI_C}}$$

Since in fixed-biasing method I_B is independent of I_C

i.e.

$$\frac{dI_B}{dI_C} = 0$$

$$\boxed{S\,(I_{CO}) = \beta + 1}$$

If β=150 S (I_{CO}) =151 which means that collector current I_C increases 151 times as much as I_{CO}. Such a large value of S (I_{CO}) makes thermal runaway, a definite possibility with this circuit.

S (V_{BE}):-

$$S(V_{BE}) = \frac{dI_C}{dV_{BE}} \quad Where\ \beta\ and\ I_{CO}\ are\ constant$$

In fixed-bias circuit the input loop equation is given by

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Differentiating w.r.t. I_C keeping β constant, we get

$$\frac{dV_{CC}}{dI_C} - \frac{1}{\beta}R_B - \frac{dV_{BE}}{dI_C} = 0$$

$$\boxed{S(V_{BE}) = \frac{-\beta}{R_B}}$$

S (β):-

$$S(\beta) = \frac{dI_C}{d\beta} \quad Where\ V_{BE}\ and\ I_{CO}\ are\ constant$$

General expression for S (β) is given by

$$S(\beta) = \frac{I_{CO} + I_B}{1 - \beta\frac{dI_B}{dI_C}}$$

Since in fixed- biasing method I_B is independent of I_C

i.e.

$$\frac{dI_B}{dI_C} = 0$$

$$\boxed{S(\beta) = I_{CO} + I_B}$$

Advantages:

- ✓ This biasing circuit is very simple as only one resistance R_B is required.
- ✓ Biasing conditions can easily be set and the calculations are simple.
- ✓ There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Disadvantages:

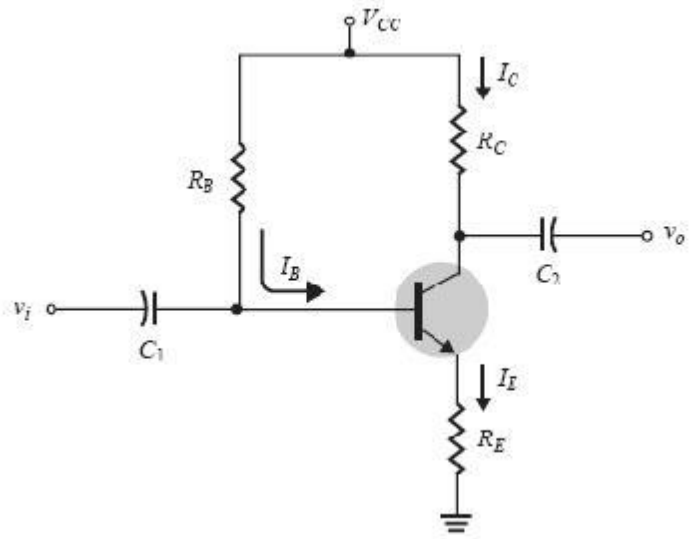
- ✓ This method provides poor stabilisation. It is because there is no means to stop a self increase in collector current due to temperature rise and individual variations. For example, if β increases due to transistor replacement, then I_C also increases by the same factor as I_B is constant.

- ✓ The stability factor is very high. Therefore, there are strong chances of thermal runaway.

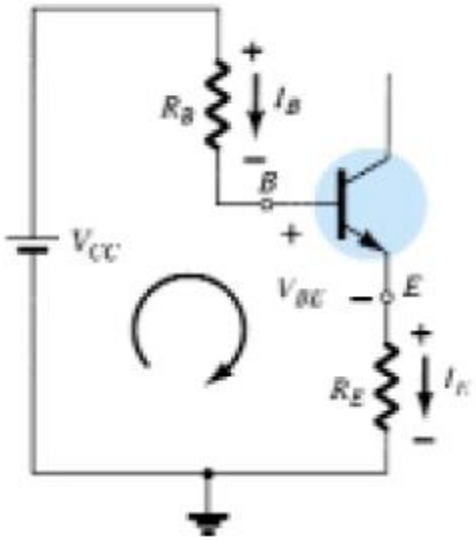
Due to these disadvantages, this method of biasing is rarely employed.

Emitter-Stabilised Bias Circuit

It can be shown that, including an emitter resistor in the fixed bias circuit improves the stability of Q point. Thus emitter bias is a biasing circuit very similar to fixed bias circuit with an emitter resistor added to it.



Input Loop



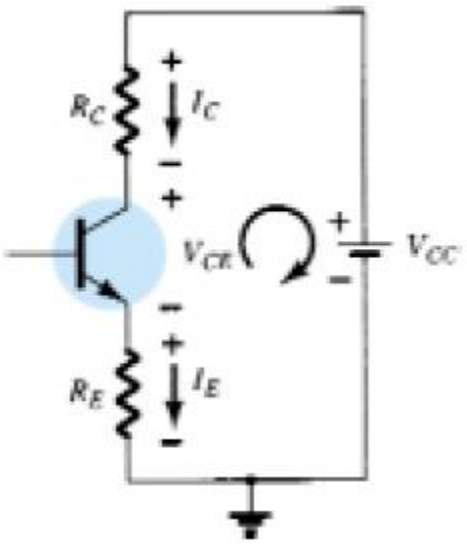
Writing KVL around the input loop we get

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}}$$

Output loop



Collector – emitter loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

IC is almost same as IE

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$

Stability Factors in Emitter-Stabilized bias Circuit

S (I_{CO}):-

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} \quad Where\ V_{BE}\ and\ \beta\ are\ constant$$

From the input circuit we get

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (I_B + I_C)\, R_E = 0$$

Differentiating above w.r.t. I_C keeping V_{BE} as constant

$$\frac{dV_{CC}}{dI_C} - R_B \frac{dI_B}{dI_C} - \frac{dV_{BE}}{dI_C} - R_E \frac{dI_B}{dI_C} - R_E = 0$$

$$-(R_B + R_E)\frac{dI_B}{dI_C} - R_E = 0$$

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_B + R_E}$$

General expression for S (I_{CO}) is given by

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta \frac{dI_B}{dI_C}}$$

So, the Stability Factor due to leakage current in Emitter-Stabilized bias Circuit is

$$\boxed{S(I_{CO}) = \frac{\beta + 1}{1 + \beta \dfrac{R_E}{R_E + R_B}}}$$

S (V_{BE}):-

$$S(V_{BE}) = \frac{dI_C}{dV_{BE}} \qquad Where\ \beta\ and\ I_{CO}\ are\ constant$$

In self-bias circuit the input loop equation is given by

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - \frac{I_C}{\beta} R_B - V_{BE} - (\beta + 1)\frac{I_C}{\beta} R_E = 0$$

Differentiating above w.r.t. I_C keeping β as constant

$$\frac{dV_{CC}}{dI_C} - \frac{R_B}{\beta} - \frac{dV_{BE}}{dI_C} - \frac{\beta + 1}{\beta} R_E = 0$$

$$-\left[\frac{R_B}{\beta} + \frac{(\beta + 1)}{\beta} R_E\right] = \frac{dV_{BE}}{dI_C}$$

So, the Stability Factor due to base emitter voltage in Emitter-Stabilized bias Circuit is

$$S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_E}$$

S (β):-

$$S(\beta) = \frac{dI_C}{d\beta} \quad Where\ V_{BE}\ and\ I_{CO}\ are\ constant$$

General expression for S (β) is given by

$$S(\beta) = \frac{I_{CO} + I_B}{1 - \beta \frac{dI_B}{dI_C}}$$

In self-bias circuit

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_B + R_E}$$

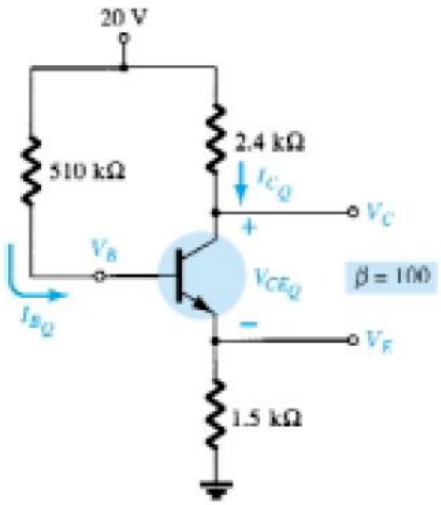
So, the Stability Factor due to current gain β in Emitter-Stabilized bias Circuit is

$$S(\beta) = \frac{I_{CO} + I_B}{1 + \beta \frac{R_E}{R_E + R_B}}$$

Numerical

For the network shown in Fig. determine the following

a) I_{B_Q} b) I_{C_Q} c) V_{CE_Q} d) V_C e) V_B



Solution:

a) Applying KVL at the input circuit

$$20 - (510K)I_B - 101 \times I_B \times (1.5K) = 0$$

$$I_{B_Q} = 29.17\mu A$$

b) $I_{C_Q} = \beta I_{B_Q} = 2.91mA$

c) $I_E = (\beta + 1)I_B = 101 \times (29.17\mu A) = 2.94mA$

$$20 - 2.91 \times 2.4 - V_{CE} - 2.94 \times 1.5 = 0$$

$$V_{CE_Q} = 8.59V$$

d) $20 - 2.91 \times 2.4 - V_C = 0$

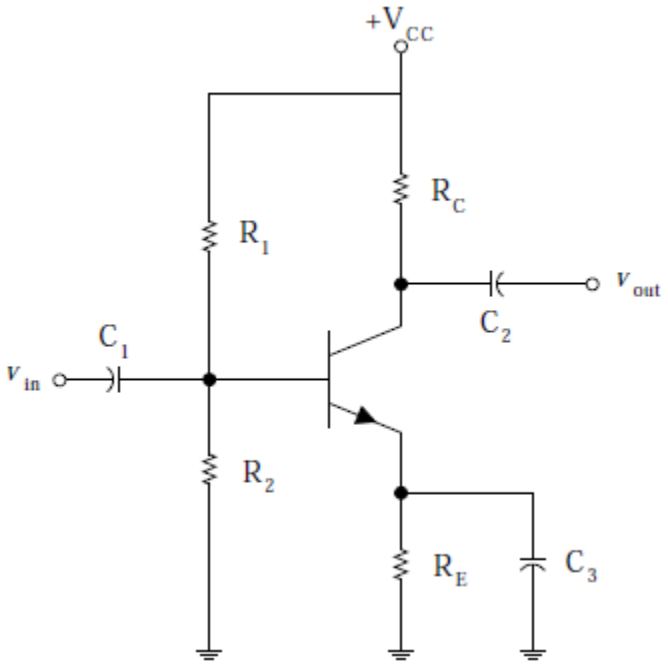
$$V_C = 13V$$

e) $V_E = I_E R_E = 2.94 \times 1.5 = 4.41V$

$$V_{BE} = V_B - V_E$$

$$V_B = V_{BE} + V_E = 0.7 + 4.41 = 5.11V$$

Voltage-divider Bias Circuit



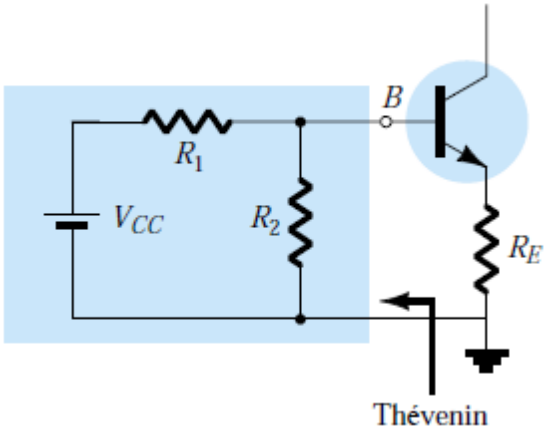
- ✓ This is the biasing circuit wherein, I_{CQ} and V_{CEQ} are almost independent of β.
- ✓ The level of I_{BQ} will change with β so as to maintain the values of I_{CQ} and V_{CEQ} almost same, thus maintaining the stability of Q point.

Two methods of analysing a voltage divider bias circuit are:

- ✓ **Exact method** – can be applied to any voltage divider circuit
- ✓ **Approximate method** – direct method, saves time and energy, can be applied in most of the circuits.

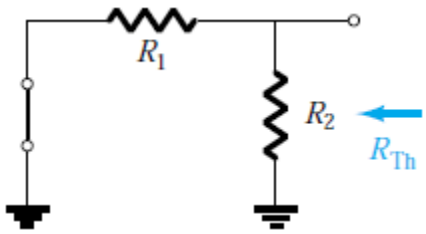
Exact method

In this method, the Thevenin equivalent network for the network to the left of the base terminal to be found.



To find R_{th}:

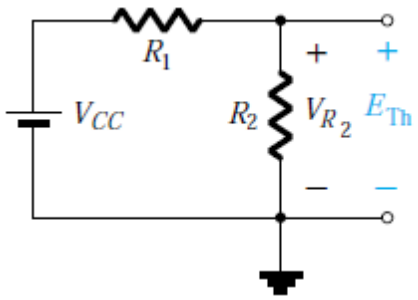
The voltage source is replaced by short-circuit equivalent as shown in figure



$$R_{th} = R_1 \parallel R_2$$

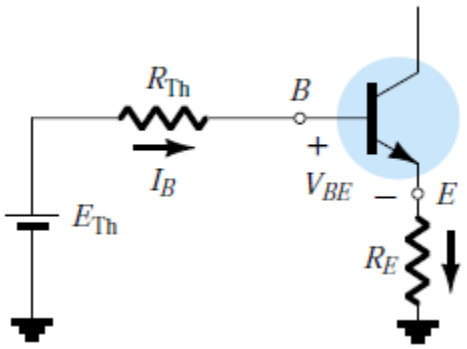
To find E_{th}:

The voltage source V_{CC} is returned to the network and the open-circuit Thevenin voltage of Fig. determined as follows:



$$E_{th} = \frac{V_{CC}R_2}{R_1 + R_2}$$

The Thevenin network is then redrawn as shown in Fig, and I_B can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:



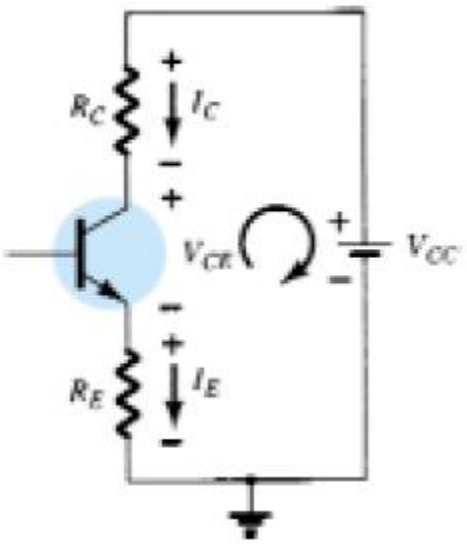
Applying KVL in the base-emitter loop

$$\mathrm{E_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0}$$

$$E_{th} - I_B R_{th} - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\boxed{I_B = \frac{E_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E}}$$

Output loop



Collector – emitter loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

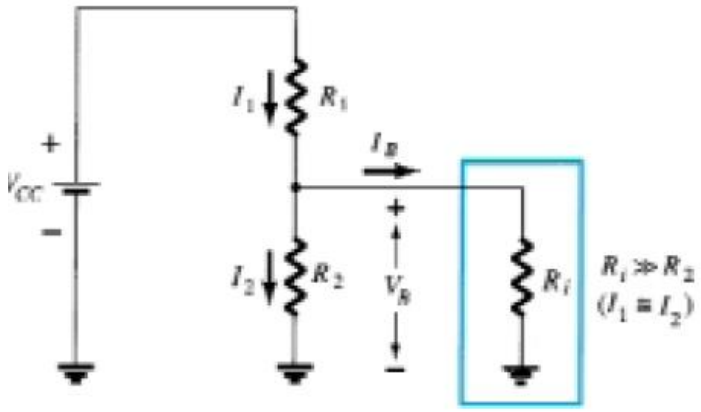
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

I_C is almost same as I_E

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Approximate method

The input section of the voltage-divider configuration can be represented by the network of Fig. The resistanceR_i is the equivalent resistance between base and ground for the transistor with an emitter resistorR_E. The reflected resistance between base +and emitter is defined by$R_i = (\beta + 1)R_E$. If R_i is much larger than the resistanceR_2, the current $I_B$will be much smaller than I_2 (current always seeks the path of least resistance) and I_2will be approximately equal toI_1. If we accept the approximation that $I_B$is essentially zero amperes compared to I_1orI_2, then $I_1 = I_2$and $R_1$and R_2can be considered series elements.



The voltage acrossR_2, which is actually the base voltage, can be determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Since $R_i = (\beta + 1)R_E \cong \beta R_E$the condition that will define whether the approximate approach can be applied will be the following:

$$\beta R_E \geq 10R_2$$

In other words, if β times the value ofR_E is at least 10 times the value ofR_2, the approximate approach can be applied with a high degree of accuracy.

Once $V_B$is determined, the level of $V_E$can be calculated from

$$V_E = V_B - V_{BE}$$

And the emitter current can be determined from

$$I_E = \frac{V_E}{R_E}$$

$$I_{C_Q} \cong I_E$$

The collector-to-emitter voltage is given by,

$$V_{CE} = V_{CC} - I_C R_C$$

Stability Factors in Voltage-divider bias Circuit

S (I_{CO}):-

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} \quad Where\ V_{BE}\ and\ \beta\ are\ constant$$

From the input circuit we get

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} - I_B R_{Th} - V_{BE} - (I_B + I_C) R_E = 0$$

Differentiating above w.r.t. I_C keeping V_{BE} as constant

$$\frac{dV_{Th}}{dI_C} - R_{Th}\frac{dI_B}{dI_C} - \frac{dV_{BE}}{dI_C} - R_E\frac{dI_B}{dI_C} - R_E = 0$$

$$-(R_{Th} + R_E)\frac{dI_B}{dI_C} - R_E = 0$$

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_{Th} + R_E}$$

General expression for S (I_{CO}) is given by

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta\frac{dI_B}{dI_C}}$$

So, the Stability Factor due to leakage current in Voltage-divider bias Circuit is

$$\boxed{S(I_{CO}) = \frac{1+\beta}{1+\beta\frac{R_E}{R_E+R_{Th}}}}$$

S (V_{BE}):-

$$S(V_{BE}) = \frac{dI_C}{dV_{BE}} \quad Where\ \beta\ and\ I_{CO}\ are\ constant$$

In Voltage-divider bias circuit the input loop equation is given by

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} - \frac{I_C}{\beta} R_{Th} - V_{BE} - (\beta+1)\frac{I_C}{\beta} R_E = 0$$

Differentiating above w.r.t. I_C keeping β as constant

$$\frac{dV_{Th}}{dI_C} - \frac{R_{Th}}{\beta} - \frac{dV_{BE}}{dI_C} - \frac{\beta+1}{\beta} R_E = 0$$

$$-\left[\frac{R_{Th}}{\beta} + \frac{(\beta+1)}{\beta} R_E\right] = \frac{dV_{BE}}{dI_C}$$

So, the Stability Factor due to base emitter voltage in Voltage-divider bias Circuit is

$$\boxed{S(V_{BE}) = \frac{-\beta}{R_{Th}+(\beta+1)R_E}}$$

S (β):-

$$S(\beta) = \frac{dI_C}{d\beta} \quad Where\ V_{BE}\ and\ I_{CO}\ are\ constant$$

General expression for S (β) is given by

$$S(\beta) = \frac{I_{CO} + I_B}{1 - \beta \frac{dI_B}{dI_C}}$$

In voltage-divider circuit

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_{Th} + R_E}$$

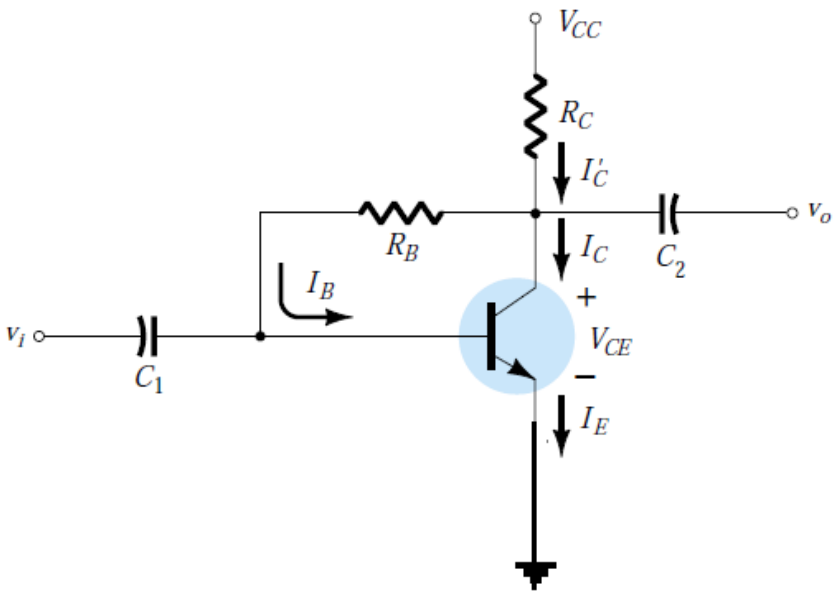
So, the Stability Factor due to current gain β in Voltage-divider bias Circuit is

$$\boxed{S(\beta) = \frac{I_{CO} + I_B}{1 + \beta \frac{R_E}{R_E + R_{Th}}}}$$

Collector-to-Base Bias

(Or Base-bias with Collector Feedback)

This circuit is like a fixed bias circuit except that base resistor R_B is returned to the collector terminal instead ofV_{CC}. It derives its name from the fact that voltage for R_B is derived from collector. There exists a negative feedback effect which tends to stabilize $I_C$against changes either as a result of change in temperature or as a result of replacement of the transistor by another one.

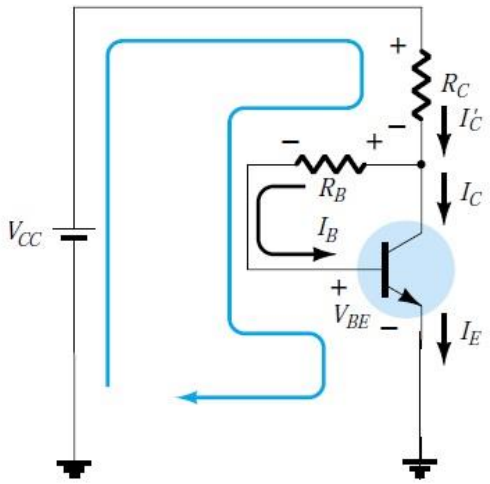


Circuit Operation

If the collector current I_C tends to increase (either due to rise in temperature or due to replacement of transistor), V_{CE} decreases due to larger voltage drop across collector resistor R_C. The result is that base current I_B is reduced. The reduced base current in turn reduces the original increase in collector current I_C. Thus a mechanism exists in the circuit which does not allow collector current I_C to increase rapidly.

Circuit Analysis

The required value of base current I_B to give zero signal collector current I_C can be determined as follows:



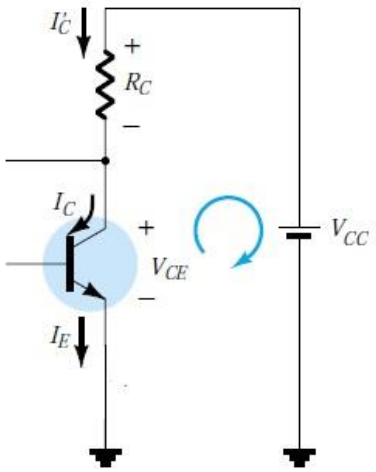
From the circuit diagram shown in Figure, applying Kirchhoff's voltage law to the input circuit, we have

$$V_{CC} - I_C{}'R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}}$$

From the output section of the circuit we have



$$V_{CE} = V_{CC} - I_C{}'R_C$$

Since $I_C{}' \cong I_C$

$$\boldsymbol{V_{CE} = V_{CC} - I_C R_C}$$

This is exactly as obtained for fixed-bias configuration.

Stability Factors in Collector-to-Base Bias

S (I_{CO}):-

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} \quad Where\ V_{BE}\ and\ \beta\ are\ constant$$

From the input circuit we get

$$V_{CC} - I_B(R_C + R_B) - V_{BE} - I_C R_C = 0$$

Differentiating above w.r.t. I_C keeping V_{BE} as constant

$$\frac{dV_{cc}}{dI_C} - (R_c + R_B)\frac{dI_B}{dI_C} - \frac{dV_{BE}}{dI_C} - R_C = 0$$

$$\frac{dI_B}{dI_C} = \frac{-R_C}{R_B + R_C}$$

General expression for S (I_{CO}) is given by

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta\frac{dI_B}{dI_C}}$$

So, the Stability Factor due to leakage current in collector-to-base bias circuit is

$$\boxed{S(I_{CO}) = \frac{1 + \beta}{1 + \beta\frac{R_C}{R_B + R_C}}}$$

Value of stability factor so obtained is less than (1+β) obtained from fixed-bias circuit. So this method provides improved stability as compared to that of fixed-bias circuit.

S (V_{BE}):-

$$S(V_{BE}) = \frac{dI_C}{dV_{BE}} \quad Where\ \beta\ and\ I_{CO}\ are\ constant$$

In collector-to-base bias circuit the input loop equation is given by

$$V_{CC} - I_B(R_C + R_B) - V_{BE} - I_C R_C = 0$$

$$V_{CC} - \frac{I_C}{\beta}(R_C + R_B) - V_{BE} - I_C R_C = 0$$

$$V_{CC} - I_C(\frac{R_C + R_B}{\beta} + R_C) - V_{BE} = 0$$

Differentiating above w.r.t. I_C keeping β as constant

$$\frac{dV_{cc}}{dI_C} - (\frac{R_c + R_B}{\beta} + R_C)\frac{dI_B}{dI_C} - \frac{dV_{BE}}{dI_C} = 0$$

So, the Stability Factor due to base emitter voltage in collector-to-base bias Circuit is

$$\boxed{S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_C}}$$

S (β):-

$$S(\beta) = \frac{dI_C}{d\beta} \quad Where\ V_{BE}\ and\ I_{CO}\ are\ constant$$

General expression for S (β) is given by

$$S(\beta) = \frac{I_{CO}+I_B}{1-\beta\frac{dI_B}{dI_C}}$$

In collector-to-base bias circuit

$$\frac{dI_B}{dI_C} = \frac{-R_C}{R_B + R_C}$$

So, the Stability Factor due to current gain β in collector-to-base bias circuit is

$$\boxed{S(\beta) = \frac{I_B + I_{CO}}{1 + \beta\frac{R_C}{R_B + R_C}}}$$

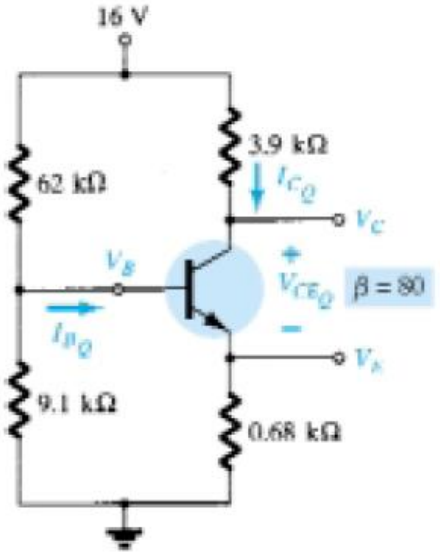
Numerical

1. For the network of Fig., determine:

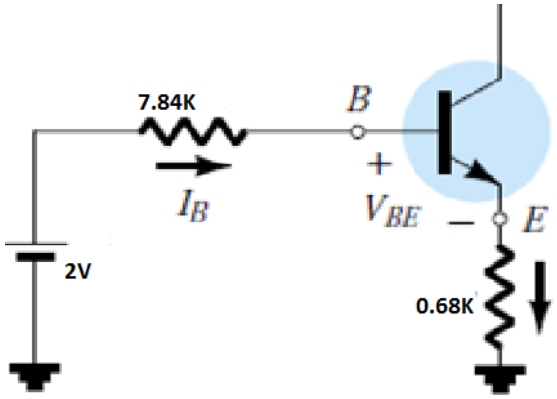
(a) $S(I_{CO})$

(b) $S(V_{BE})$

(c) $S(\beta)$ Using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than$\beta(T_1)$.



a) Applying Thevenin equivalent results



From the input circuit we get

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} - I_B R_{Th} - V_{BE} - (I_B + I_C)\, R_E = 0$$

$$2V - I_B(7.84K) - 0.7 - (I_C + I_B)(0.68K) = 0$$

Differentiating above w.r.t. I_C keeping V_{BE} as constant

$$\frac{dV_{Th}}{dI_C} - R_{Th}\frac{dI_B}{dI_C} - \frac{dV_{BE}}{dI_C} - R_E\frac{dI_B}{dI_C} - R_E = 0$$

$$(-7.84K)\frac{dI_B}{dI_C} - (0.68K) - (0.68K)\frac{dI_B}{dI_C} = 0$$

$$-(8.52K)\frac{dI_B}{dI_C} = 0.68K$$

$$\frac{dI_B}{dI_C} = -7.98 \times 10^{-2}$$

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta\frac{dI_B}{dI_C}}$$

$$= \frac{81}{1 + 80 \times 7.98 \times 10^{-2}} = 10.96$$

b) From the input circuit,

$$V_{Th} - \frac{I_C}{\beta}R_{Th} - V_{BE} - (\beta + 1)\frac{I_C}{\beta}R_E = 0$$

$$2 - \frac{I_C}{80}(7.84K) - V_{BE} - \frac{81 \times (0.68K)}{80}I_C = 0$$

By, differentiation

$$-(0.098K) - \frac{dV_{BE}}{dI_C} - (0.68K) = 0$$

$$S(V_{BE}) = -1.28 \times 10^{-3}s$$

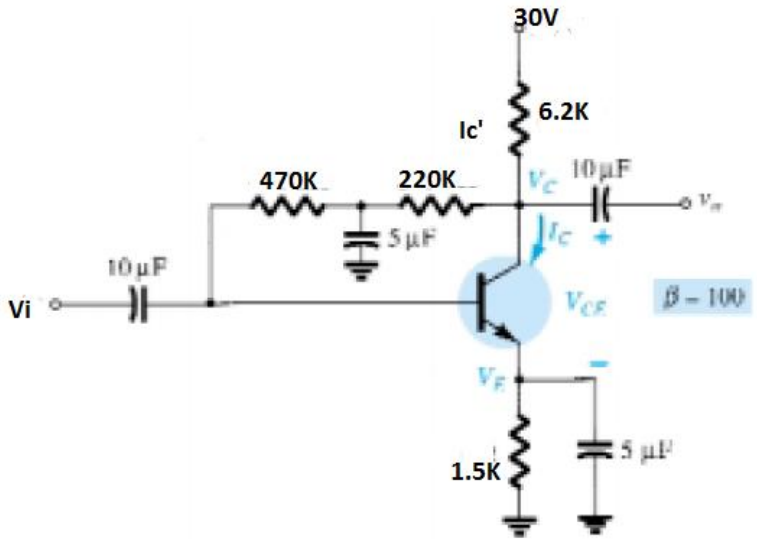
c) $\beta_1 = 80$ $\beta_2 = 80$

$I_{C_1} = 1.653mA$ $I_{C_2} = 1.698mA$

$$S(\beta) = \frac{1.698 - 1.653}{100 - 80} = 2.25 \times 10^{-6}A$$

2. For the voltage feedback network of Fig., determine:

a) I_C
b) V_C
c) V_E
d) V_{CE}



a) $30 - (6.2K)I_C{}' - (470K + 220K)I_B - 0.7 - (1.5K)I_E = 0$

$$30 - (6.2K)(\beta + 1)I_B - (690K)I_B - 0.7 - (1.5K)(\beta + 1)I_B = 0$$

$$30 - (6.2K) \times 101I_B - (690K)I_B - 0.7 - (1.5K) \times 101I_B = 0$$

$$I_B = 19.96\mu A$$

$$I_C = \beta I_B = 1.99mA$$

b) $30 - (6.2K){I_C}' - V_C = 0$

$$V_C = 17.49V$$

c) $V_E = I_E R_E = 2.026 \times 1.5 = 3.024V$

d) $V_{CE} = V_C - V_E = 14.466V$

Unit 2

MOS
Field-Effect Transistor

Prepared by:

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References: 1. "Electronic Devices and Circuits"

J.B. Gupta

2. "Semiconductor physics and devices"

Donald A. Neaman

3. "Microelectronics Circuits"

Sedra and Smith

Field Effect Transistor

The field effect transistor is a semiconductor device, which depends for its operation on the control of current by an electric field. There are two of field effect transistors:

- ✓ JFET (Junction Field Effect Transistor)
- ✓ MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

The FET has several advantages over conventional transistor.

- ✓ In a conventional transistor, the operation depends upon the flow of majority and minority carriers. That is why it is called bipolar transistor. In FET the operation depends upon the flow of majority carriers only. It is called unipolar device.

- ✓ The input to conventional transistor amplifier involves a forward biased PN junction with its inherently low dynamic impedance. The input to FET involves a reverse biased PN junction hence the high input impedance of the order of Mega ohm.

- ✓ It is less noisy than a bipolar transistor.

- ✓ It exhibits no offset voltage at zero drain current.
- ✓ It has thermal stability.

- ✓ It is relatively immune to radiation

Operation of JFET

Consider a sample bar of N-type semiconductor. This is called N-channel and it is electrically equivalent to a resistance as shown in **fig. 1**.

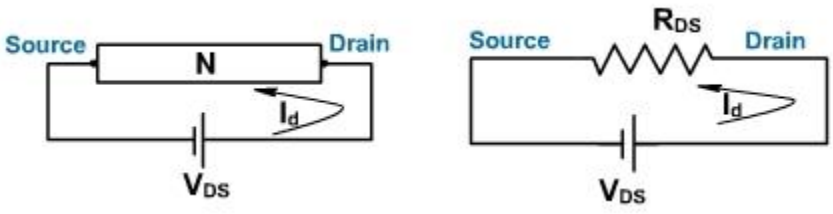


Fig. 1

Ohmic contacts are then added on each side of the channel to bring the external connection. Thus if a voltage is applied across the bar, the current flows through the channel.

The terminal from where the majority carriers (electrons) enter the channel is called source designated by S. The terminal through which majority carriers leave the channel is called drain and designated by D. For an N-channel device, electrons are the majority carriers. Hence the circuit behaves like a dc voltage V_{DS} applied across a resistance R_{DS}. The resulting current is the drain current I_D. If V_{DS} increases, I_D increases proportionally.

Now on both sides of the n-type bar heavily doped regions of p-type impurity have been formed by any method for creating pn junction. These impurity regions are called gates (gate1 and gate2) as shown in **fig. 2**.

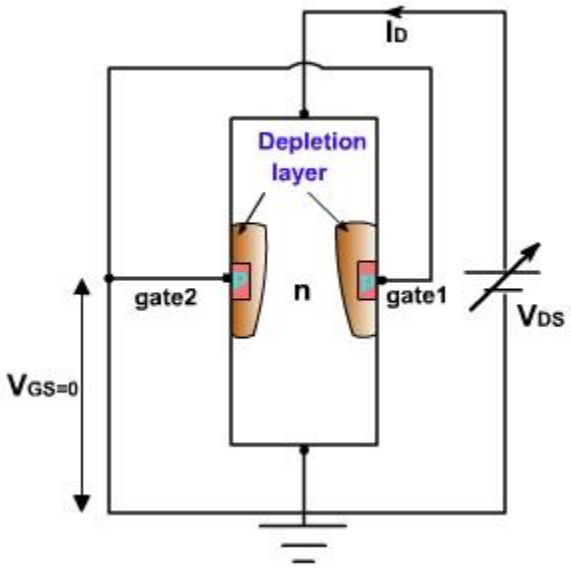


Fig. 2

Both the gates are internally connected and they are grounded yielding zero gate source voltage (V_{GS} =0). The word gate is used because the potential applied between gate and source controls the channel width and hence the current.

As with all PN junctions, a depletion region is formed on the two sides of the reverse biased PN junction. The current carriers have diffused across the junction, leaving only uncovered positive ions on the n side and negative ions on the p side. The depletion region width increases with the magnitude of reverse bias. The conductivity of this channel is normally zero because of the unavailability of current carriers.

The potential at any point along the channel depends on the distance of that point from the drain, points close to the drain are at a higher positive potential, relative to ground, then points close to the source. Both depletion regions are therefore subject to greater reverse voltage near the drain. Therefore the depletion region width increases as we move towards drain. The flow of electrons from source to drain is now restricted to the narrow channel between the no conducting depletion regions. The width of this channel determines the resistance between drain and source.

Characteristics of JFET

Consider now the behavior of drain current I_D vs drain source voltage V_{DS}. The gate source voltage is zero therefore $V_{GS}= 0$. Suppose that V_{DS} is gradually linearly increased linearly from 0V. I_D also increases.

Since the channel behaves as a semiconductor resistance, therefore it follows ohm's law. The region is called ohmic region, with increasing current, the ohmic voltage drop between the source and the channel region reverse biased the junction, the conducting portion of the channel begins to constrict and I_D begins to level off until a specific value of V_{DS} is reached, called the **pinch of voltage V_P**.

At this point further increase in V_{DS} does not produce corresponding increase in I_D. Instead, as V_{DS} increases, both depletion regions extend further into the channel, resulting in a no more cross section, and hence a higher channel resistance. Thus even though, there is more voltage, the resistance is also greater and the current remains relatively constant. This is called pinch off or saturation region. The current in this region is maximum current that FET can produce and designated by I_{DSS}. (Drain to source current with gate shorted).

As with all pn junctions, when the reverse voltage exceeds a certain level, avalanche breakdown of pn junction occurs and I_D rises very rapidly as shown in **fig. 3**.

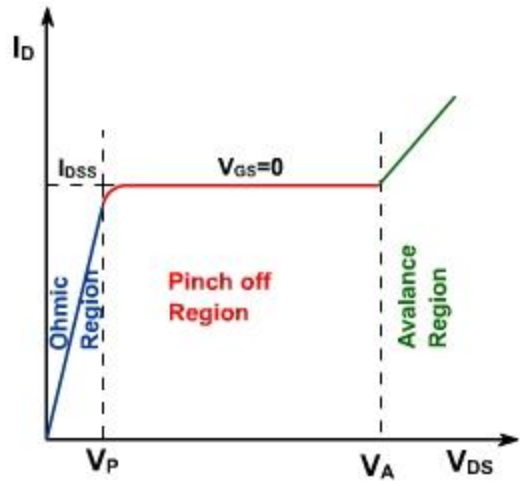


Fig. 3

Consider now an N-channel JFET with a reverse gate source voltage as shown in **fig. 4**.

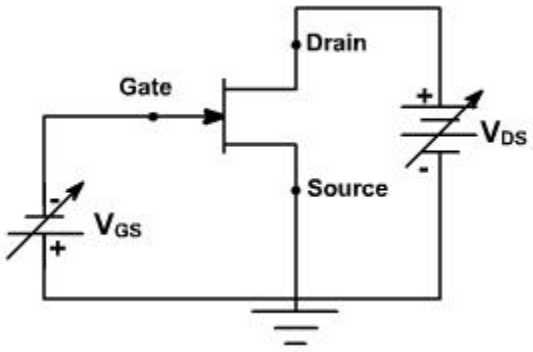


Fig.4

The additional reverse bias, pinch off will occur for smaller values of $|V_{DS}|$, and the maximum drain current will be smaller. A family of curves for different values of V_{GS} (negative) is shown in **fig. 5**.

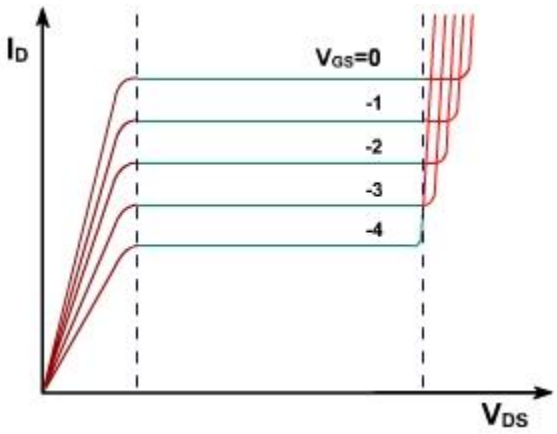


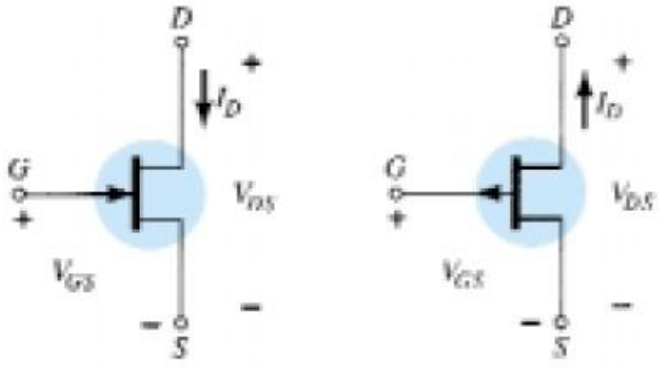
Fig.5

When the gate voltage is negative enough, the depletion layers touch each other and the conducting channel pinches off (disappears). In this case the drain current is cut off. The gate voltage that produces cut off is symbolized V_{GS} (off). It is same as pinch off voltage.

Since the gate source junction is a reverse biased silicon diode, only a very small reverse current flows through it. Ideally gate current is zero. As a result, all the free electrons from the source go to the drain i.e. $I_D = I_S$. Because the gate draws almost negligible reverse current the input resistance is very high 10's or 100's of M ohm. Therefore where high input impedance is required, JFET is preferred over BJT. The disadvantage is less control over output current i.e. FET takes larger changes in input voltage to produce changes in output current. For this reason, JFET has less voltage gain than a bipolar amplifier.

Symbol of JFET

The graphic symbols for the n-channel and p-channel JFETs are provided in Fig. Note that the arrow is pointing in for the n-channel device of Fig. to represent the direction in which I_G would flow if the p-n junction were forward-biased. For the p-channel device the only difference in the symbol is the direction of the arrow.



(a) n-channel (b) p-channel

JFET Temperature Effects

It is possible to bias the JFET such that it exhibits a zero temperature co-efficient i.e. drain current is independent of temperature. There are two mechanisms for controlling the temperature sensitivity of the conduction of a JFET channel.

- ✓ Decreasing the depletion region width at the channel-gate pn junction with increase in temperature, this result in increase in channel thickness.
- ✓ Decrease in carrier mobility with increase in temperature.

Increase in channel thickness with increasing temperature makes drain current I_D to increase. Another way of looking in to the situation is that, V_P increase in magnitude with increase in temperature. V_P has a positive temperature coefficient of about 2.2 mV/^{0}C.

The second factor, i.e. decrease in carrier mobility with increase in temperature make channel conductivity to decrease with increase in temperature. The result is that, the drain current decreases with increase in temperature.

So, we have two distinct mechanism effecting the $I_D$as a function of temperature. Since both these mechanisms occur simultaneously, it is possible to bias the JFET so as to exhibit zero temperature co-efficient. Thus the JFET have higher thermal stability as thermal runaway does not occur in JFET.

JFET Parameters

1. AC drain resistance

It is defined as the ratio of change in V_{DS} to the change in drain current at constant gate-source voltageV_{GS}. It is denoted as r_d.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad at\ constant V_{GS}$$

It is also called dynamic drain resistance and its value is very large from 10 KΩ to 1 MΩ.

2. Transconductance

The control that V_{GS} has over drain current I_D is measured by transconductance. It is denoted as g_m. It may be defined as ratio of change in drain current (I_D) to the change in gate-source voltage (V_{GS}) at constant drain-source voltage (V_{DS}).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big| V_{DS} = constant$$

It is also called the forward trans-admittance (y_{fs}) or forward transconductance (g_{fs}). It is measured in $^{mA}/_{V}$ or milli siemens.

3. Amplification Factor

It may be defined as ratio of change in drain-source voltage (V_{DS}) to the change in gate-source voltage (V_{GS}) at constant drain current (I_D). It is denoted as μ.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big| I_D = constant$$

Relationship among JFET parameters

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D} \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boldsymbol{\mu = r_d \times g_m}$$

JFET Equation

The drain current I_D of JFET described by the following equation

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

MOSFET

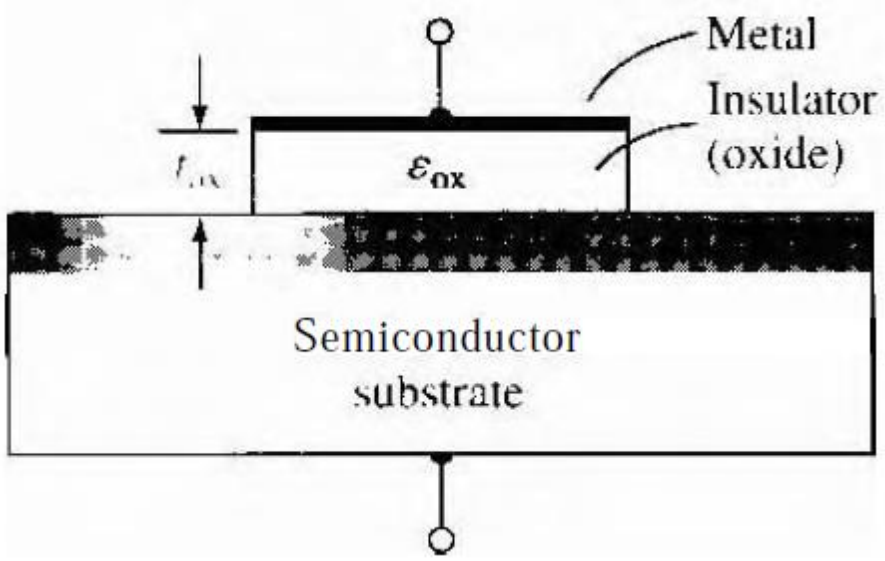
INTRODUCTION

- ✓ The metal-oxide-semiconductor field effect transistor (MOSFET) became a practical reality in the 1970s.
- ✓ The MOSFET compared to BJTs, can be made very small i.e. it occupies a very small area on an IC chip.
- ✓ Since digital circuits can be designed using only MOSFETs, with essentially no resistors or diodes required, high density VLSI circuits, including microprocessors and memories can be fabricated.
- ✓ The MOSFET has made possible the handheld calculator, the powerful personal computer and the laptop computer.

MOS STRUCTURE

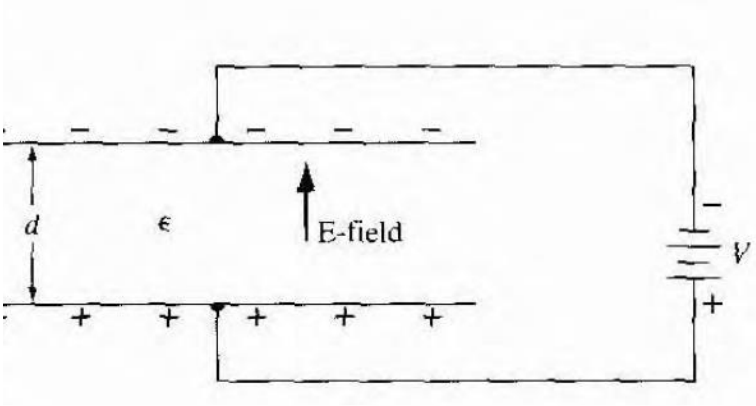
MOS Capacitor

- ✓ The heart of the MOSFET is the metal-oxide-semiconductor capacitor.
- ✓ The metal may be aluminium or some other type of metal.
- ✓ In most cases, the metal is replaced by a high conductivity polycrystalline silicon layer deposited on oxide.
- ✓ However the term metal is usually still used in referring to MOSFETs.
- ✓ The parameter t_{ox} is the thickness of the oxide and $\in_{ox}$ is the oxide permittivity.

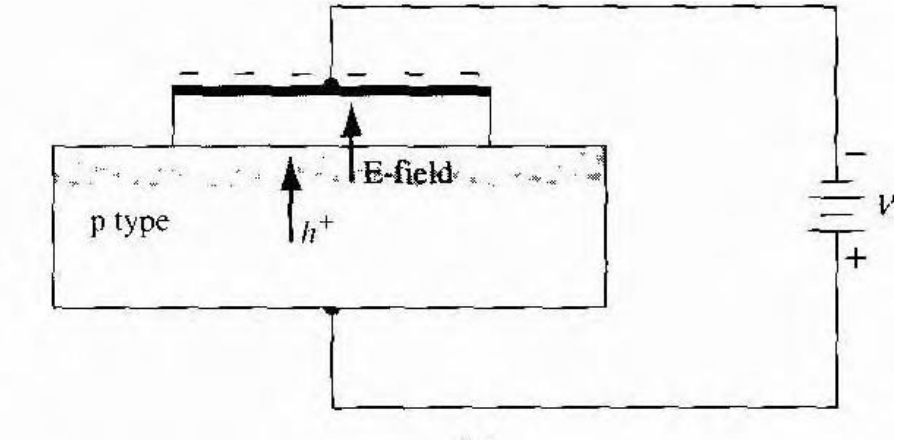


Parallel plate capacitor

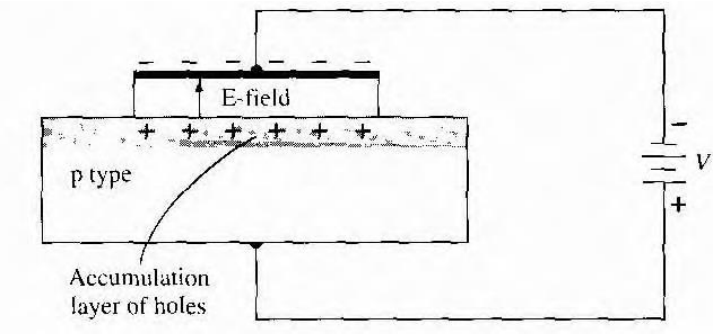
- ✓ The physics of MOS structure can be explained with the aid of a simple parallel plate capacitor.
- ✓ Figure shows a parallel plate capacitor with the top plate at negative voltage w.r.t. the bottom plate.
- ✓ An insulator material separates two plates.
- ✓ With this bias, a negative charge exists on the top plate, a positive charge exists on the bottom plate and electric field is induced between the two plates.



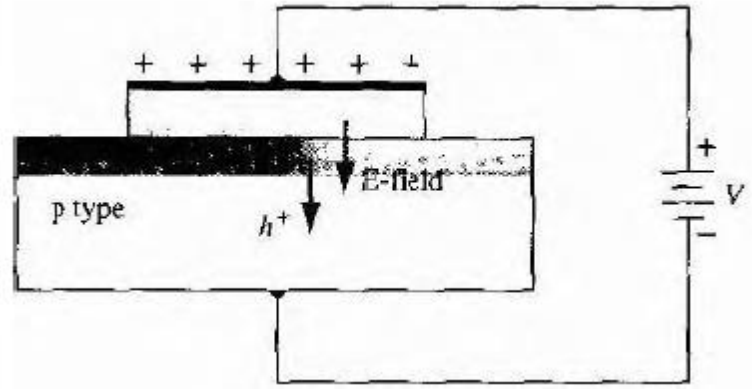
MOS capacitor with p-type Substrate



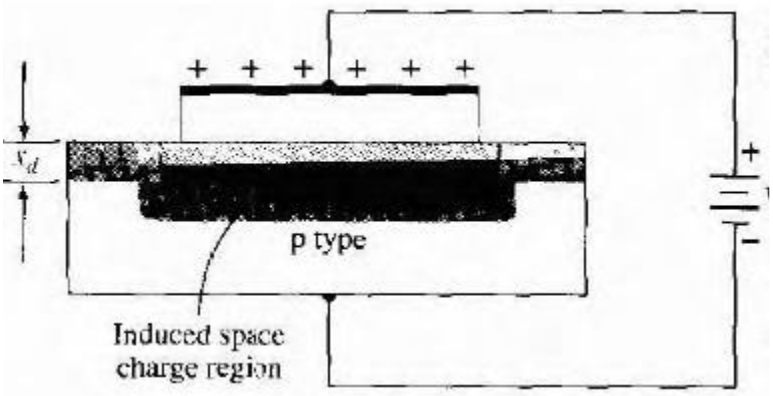
- ✓ Figure shows an MOS capacitor with a p-type semiconductor substrate.
- ✓ The top metal gate is at a negative voltage with respect to the semiconductor substrate.
- ✓ From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced with the direction shown in the figure.
- ✓ If the electric field were to penetrate into the semiconductor, the majority carrier holes would experience a force toward the oxide-semiconductor interface.



- ✓ An ***accumulation layer of holes*** in the oxide-semiconductor junction corresponds to the positive charge on the bottom "plate" of the MOS capacitor.
- ✓ Figure shows the same MOS capacitor in which the polarity of the applied voltage is reversed.



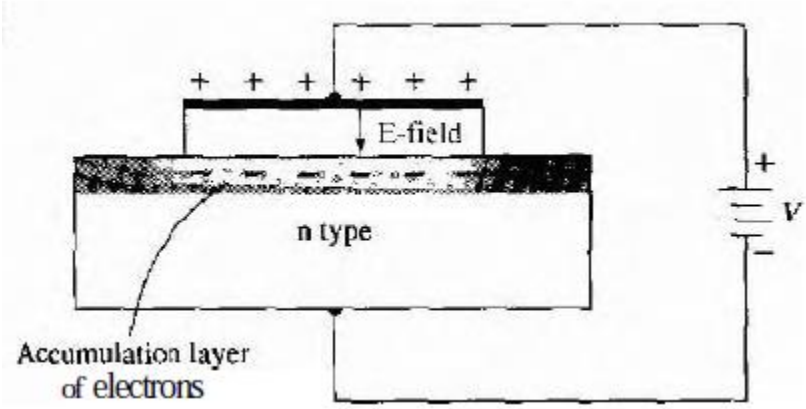
- ✓ A positive charge now exists on the top metal plate and the induced electric field is in the opposite direction as shown.
- ✓ If the electric field penetrates the semiconductor in this case, majority carrier holes will experience a for away from the oxide-semiconductor interface.
- ✓ As the holes are pushed away the interface, a negative space charge region is created because of the fixed acceptor impurity atoms.
- ✓ The negative charge in the induced depletion region corresponds to the negative charge on the bottom "plate" of the MOS capacitor.



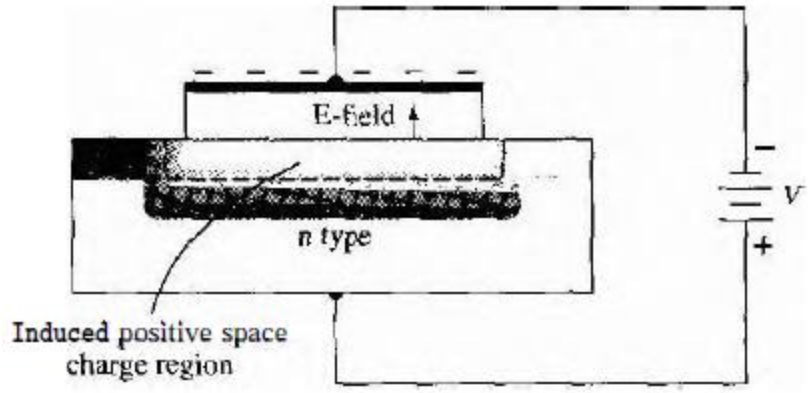
- ✓ When a large positive voltage is applied to the gate, the magnitude of the induced electric field increases.
- ✓ Minority carrier electrons are attracted to the oxide-semiconductor interface.
- ✓ This region of minority carrier electrons is called an *electron inversion layer*.

MOS capacitor with n-type Substrate

- ✓ The top metal plate is at positive voltage w.r.t. the semiconductor interface.
- ✓ A positive charge is created on the top plate and electric field is induced.
- ✓ In this situation an accumulation layer of electrons is induced in the n-type semiconductor.



- ✓ When a negative voltage is applied to the gate terminal, a positive space charge region is induced in the n-type substrate by the induced electric field.
- ✓ When a large negative voltage is applied, a region of positive charge is created at the oxide semiconductor interface.
- ✓ This region of minority carrier holes is called *hole inversion layer*.

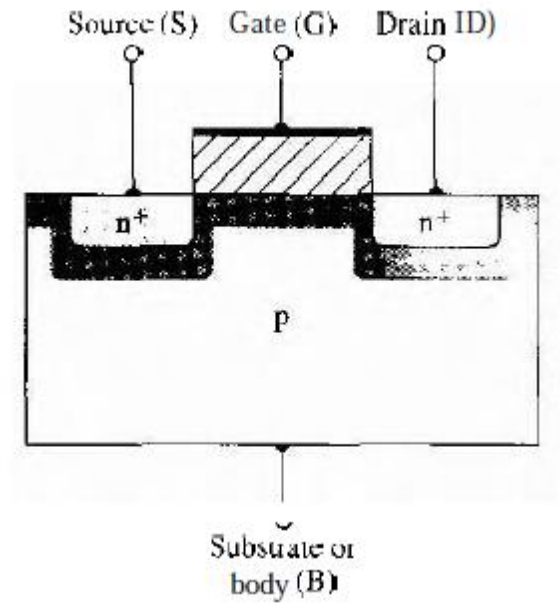


Enhancement-mode MOSFET

- ✓ The term enhancement mode means that a voltage must be applied to the gate to create an inversion layer.
- ✓ For MOS capacitor with a p-type substrate, a positive gate voltage must be applied to create the electron inversion layer.
- ✓ For MOS capacitor with a n-type substrate, a negative gate voltage must be applied to create the hole inversion layer.

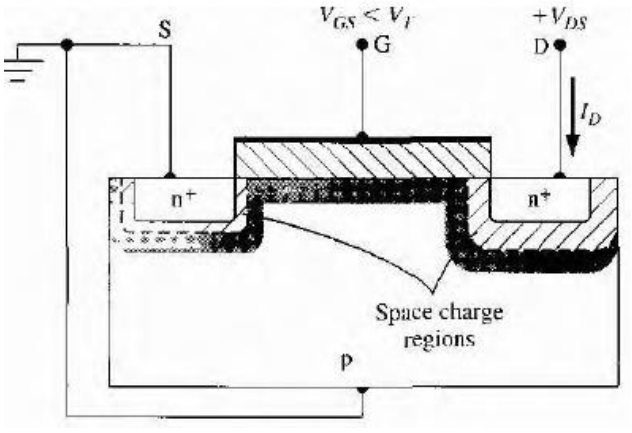
n-channel Enhancement-mode MOSFET

The gate, oxide and p-type substrate regions are same as those of a MOS capacitor. In addition, we have now two n-regions, called source terminal and drain terminal. The current in a MOSFET is the result of the flow of charge in the inversion layer, also called channel-region, adjacent to the oxide-semiconductor interface. The channel length of a typically integrator circuit MOSFET is less than 1µm which means MOSFETs are small devices. The oxide thickness t_{ox} is typically in the order of $400A^0$ or less. With zero bias applied to the gate, the source and drain terminals are separated by p-regions. This is equivalent to two back to back diodes. The current in this case is essentially zero. If large enough positive gate voltage is applied, an electron inversion layer is created at the oxide-semiconductor interface and this layer connects n-source to n-drain. A current can be generated between the source and drain terminals. Since a voltage must be applied to the gate to create the inversion charge, this transistor is called enhancement mode MOSFET. Since carriers in the inversion layer are electrons, this device is also called an n-channel MOSFET (NMOS). The source terminal supplies the electrons that flow through the channel and the drain terminal allows the carriers to drain from the channel. For n-channel MOSFET, electrons flow from the source to the drain with an applied drain-to-source voltage which means conventional current enters the drain and leaves the source. The magnitude of current is a function of the amount of the charge in the inversion layer, which in turn is a function of the applied gate voltage. Since the gate terminal is separated from the channel by an oxide or insulator, there is no gate current. Similarly, since the channel and substrate are separated by a space-charge region, there is no current through the substrate.

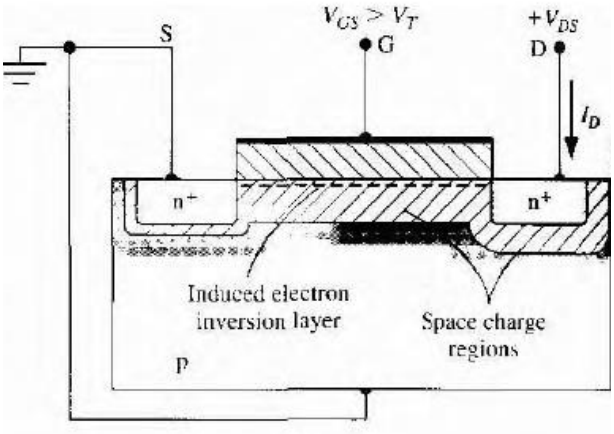


V-I Characteristics-NMOS Device

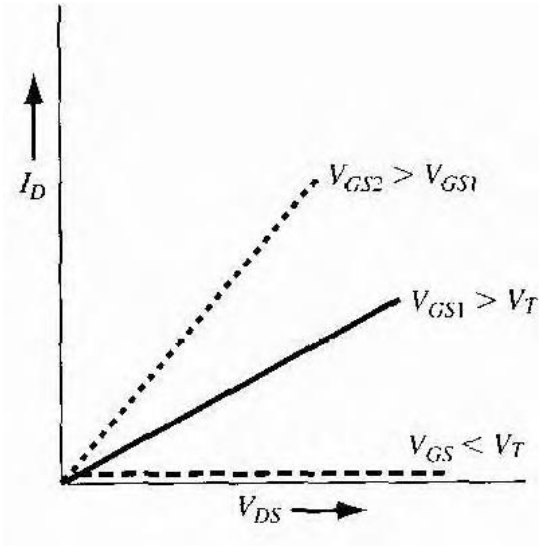
The threshold voltage of the n-channel MOFET, denoted asV_{TN}, is defined as the applied gate voltage needed to create an inversion layer. In simple terms, the threshold voltage is the gate voltage required to turn on the transistor. For the n-channel E-MOSFET, the threshold voltage is positive because a positive gate voltage is required to create the inversion layer. If the gate voltage is less than threshold voltage, the current in the device is essentially zero.



If the gate voltage is greater than the threshold voltage a drain-to-source current is generated as drain-to-source voltage is applied. The gate and drain voltages are measured w.r.t. the source. The drain-to-source voltage is less than threshold voltage and there is a small drain-to-source voltage. There is no electron in the inversion layer, the drain-to-substrate pn junction is reverse biased and the drain current is zero. If the applied gate voltage is greater than the threshold voltage an electron inversion layer is created. When a small drain voltage is applied, electrons in the inversion layer flow from source to positive drain terminal. The conventional current enters the drain terminal and leaves the source terminal. Note that positive drain voltage creates a reverse-biased drain-to-substrate pn junction, so current flows through the channel region and not through a pn junction.



The I_D versus V_{DS} characteristics, for small values of V_{DS}, are shown in Figure



When$V_{GS} < V_{TN}$, the drain current is zero. As V_{GS} becomes larger than V_{TN}, channel inversion charge density increases, which increases the channel conductance.

Figure shows the basic MOS structure for the case when $V_{GS} > V_{TN}$, and the applied V_{DS} voltage is small. The thickness of the inversion channel layer in the figure qualitatively indicates the relative charge density, which is essentially constant along the entire channel length for this case. The corresponding I_D versus V_{DS} curve is shown in the figure.

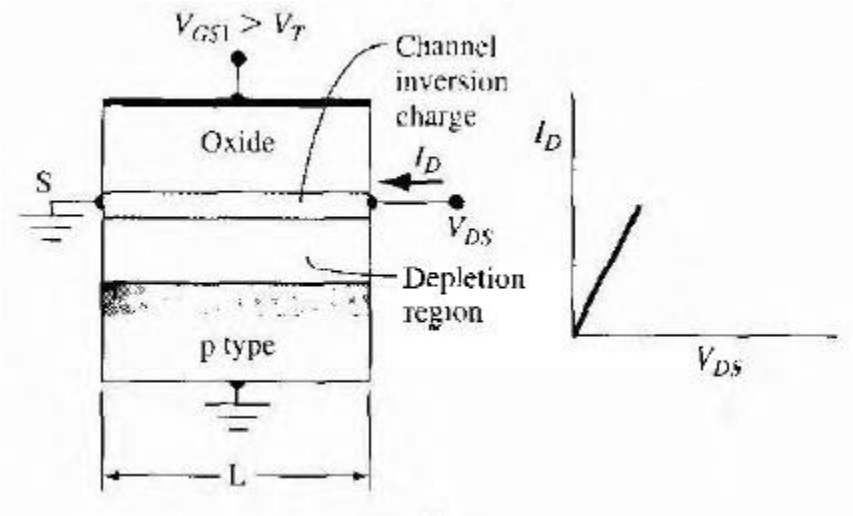
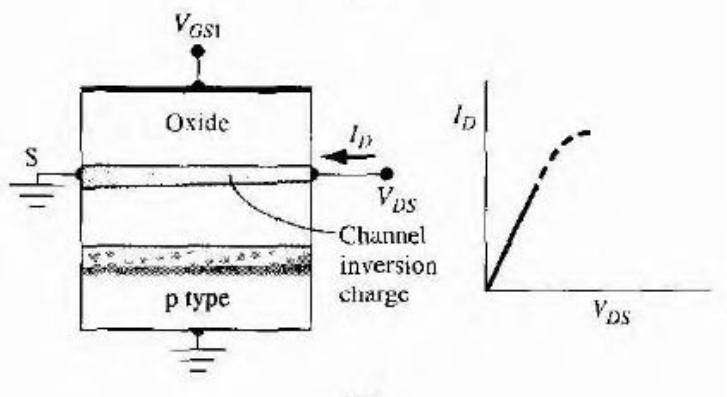


Figure shows the situation when the V_{DS} value increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases. The incremental conductance of the channel at the drain decreases, which means that the slope of the I_D versus V_{DS} curve will decrease. This effect is shown in the I_D versus V_{DS} curve in the figure.

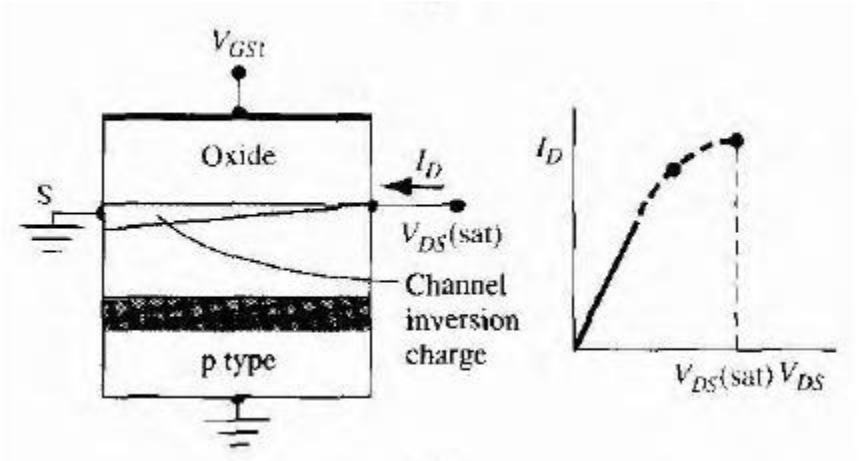


When V_{DS} increases to the point where the potential drop across the oxide at the drain terminal is equal to V_{TN}, the induced inversion charge density is zero at the drain terminal. This effect is schematically shown in Figure. At this point, the incremental conductance at the drain is zero, which means that the slope of the I_D versus V_{DS} curve is zero. We can write

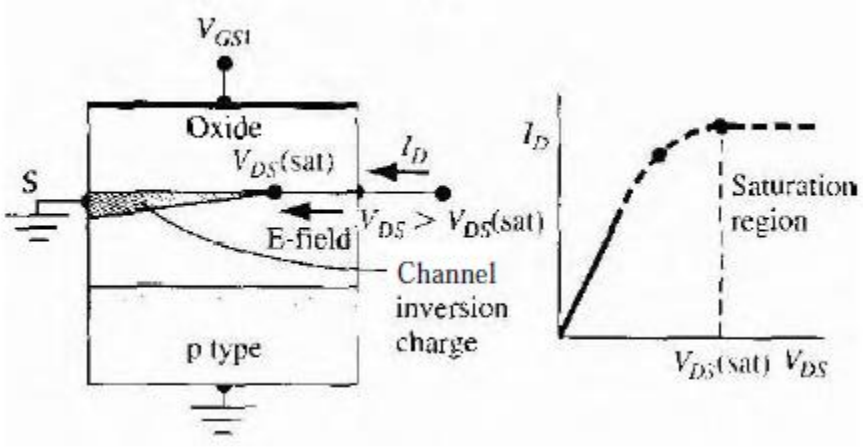
$$V_{GS} - V_{DS}(sat) = V_{TN}$$

Or, $$\boxed{V_{DS}(sat) = V_{GS} - V_{TN}}$$

where V_{DS}(sat) is the drain-to-source voltage producing zero inversion charge density at the drain terminal.



When V_{DS} becomes larger than the V_{DS} (sat) value, the point in the channel at which the inversion charge is just zero moves toward the source terminal. In this case, electrons enter the channel at the source, travel through the channel toward the drain, and then, at the point where the charge goes to zero, the electrons are injected into the space charge region where they are swept by the E-field to the drain contact. If we assume that the change in channel length is small compared to the original length, then the drain current will be a constant for V_{DS} > V_{DS} (sat). The region of the I_D versus V_{DS} characteristic is referred to as the ***saturation region.*** Figure shows this region of operation.



As the applied gate-to-source voltage changes, the I_D versus V_{DS} curve changes. The region for which $V_{DS} < V_{DS}(sat)$ is known as the ***non-saturation or triode region***. The ideal current-voltage characteristics in this region are described by the equation.

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - {V_{DS}}^2]$$

In the saturation region, the ideal current-voltage characteristics in this region are described by the equation.

$$I_D = K_n(V_{GS} - V_{TN})^2$$

K_n is the transconductance parameter which is given by:

$$K_n = \frac{\mu_n C_{ox} W}{2L}$$

Where,

$$\mu_n = \text{mobility of electrons}$$

C_{ox} = oxide capacitance

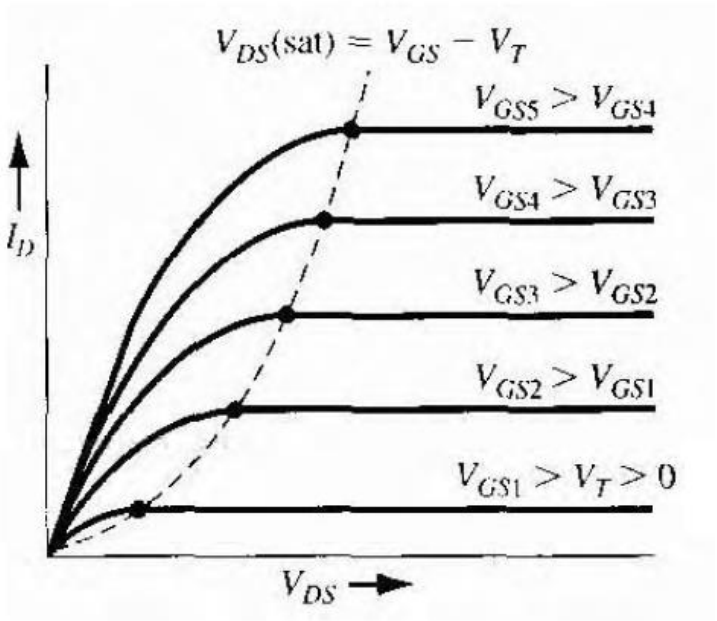
W= width of the channel

L= length of the channel

K_n' = process conduction parameter

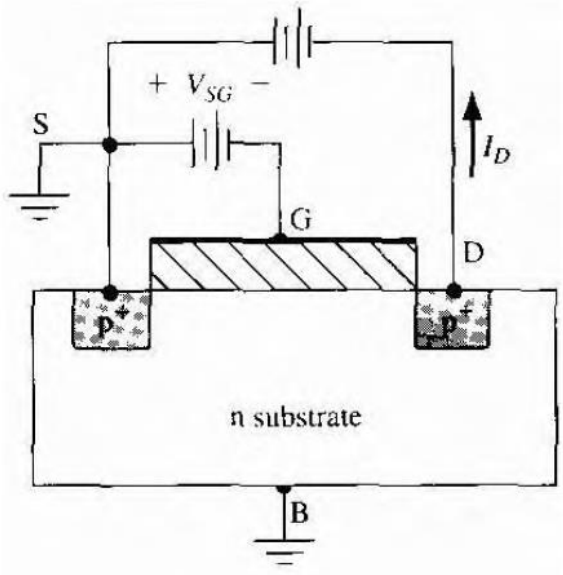
$$\boxed{K_n' = \mu_n C_{ox}}$$

$$\frac{W}{L} = aspect\ ratio$$



p-channel Enhancement-mode MOSFET

The substrate is now n-type and the source and drain areas are p-type. The operation of p-channel device is same as n-channel device, except the hole is the charge carrier rather than the electron. A negative gate bias is required to induce an inversion layer of holes in the channel region directly under the oxide. The threshold voltage for p-channel device is denoted as V_{TP}. Since the threshold voltage is defined as the gate voltage required to induce the inversion layer, then $V_{TP} < 0$ for p-channel enhancement-mode device.



Once the inversion layer has been created, the p-type source region is the source of the charge carrier so that holes flow from the source to drain. A negative drain voltage is therefore required to induce an E-field in the channel forcing the holes to move from the source to drain. The conventional current direction, then for pMOS transistor is in to the source and out of drain. The voltage polarities and current direction are the reverse of those in the n-channel device. We may note the change in the subscript notation for this device. $V_{SD}(sat)$ the drain-to-source voltage producing zero inversion charge density at the drain terminal is given by

$$V_{SD}(sat) = V_{SG} + V_{TP}$$

The ideal current-voltage characteristics in non-saturation region are described by the equation.

$$I_D = K_n[2(V_{SG} + V_{TP})V_{SD} - {V_{SD}}^2]$$

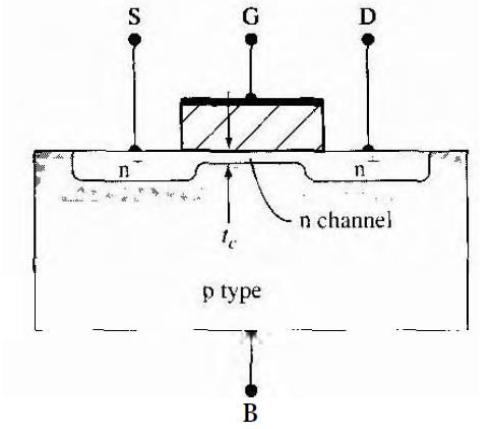
In the saturation region, the ideal current-voltage characteristics in this region are described by the equation.

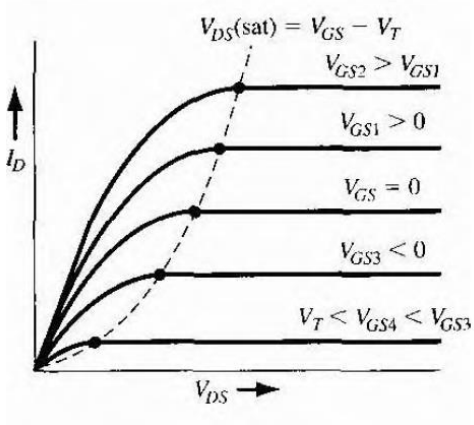
$$I_D = K_n(V_{SG} + V_{Tp})^2$$

Depletion-mode MOSFET

n-channel DMOSFET

When zero volts applied to the gate, an n-channel region or inversion layer exists under the oxide. Since an n-region connects the n-source and n-drain, a drain-to-source current may be generated in the channel even with zero gate voltage. The term depletion mode means that a channel exists even at zero gate voltage. A negative gate voltage must be applied to the n-channel D-MOSFET to turn the device off. A negative gate voltage induces a space charge region under the oxide, thereby reducing the thickness of the n-channel oxide. The reduced thickness decreases the channel conductance, which in turn reduces the drain current. The more negative the gate voltage the less is the drain current.





D-MOSFET Vs. E-MOSFET

D-MOSFET	E-MOSFET
✓ Normally ON MOSFET ✓ Already there is a channel in case of D-MOSFET. ✓ Increasing the magnitude of gate bias decreases the current. ✓ It is normally conducting but becomes non conducting as the carriers are depleted or pulled from the channel by applying voltage. ✓ The device is normally ON, we need to provide bias to turn off or pinch off the channel.	✓ Normally OFF MOSFET ✓ There is no channel in first initially. ✓ Increasing the magnitude of gate bias increases the current. ✓ It is normally non conducting but becomes conducting when the channel is enhanced by applying voltage. ✓ To turn ON the channel, we need to provide bias the gate higher than the threshold voltage.

N-channel Vs. P- channel MOSFET

- ✓ P-channel is much easier and cheaper to produce than N-channel device.
- ✓ N-channel MOSFET is smaller for the same complexity than that of P-channel MOSFET.
- ✓ N-channel MOSFET has faster switching operation than P-channel MOSFET.
- ✓ P-channel occupies larger area than N-channel for given drain current rating because the electron mobility is 2.5 times more than that of holes.
- ✓ The drain resistance of P-channel MOSFET is three times higher than that of an identical N-channel MOSFET.

Numericals

1. Use the expression for operation in triode region to show that an N-channel MOSFET operated with an overdrive voltage $V_{OV} = V_{GS} - V_{tN}$ and having small V_{DS} across it behaves approximately as a linear resistance,

$$r_{DS} = \frac{1}{[K_n' \frac{W}{L} V_{OV}]}$$

Obtained for a device having $K_n' = 1000\ \mu A/V^2$ and $\frac{W}{L} = 10$; when operated with an overdrive voltage of 0.5V.

Solution:

In triode region,

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - {V_{DS}}^2]$$

Taking, ${V_{DS}}^2$ very negligible due to very small value,

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS}]$$

$$r_{DS} = (\frac{\partial I_D}{\partial V_{DS}})^{-1} \Big| V_{DS} = constant$$

$$\frac{\partial I_D}{\partial V_{DS}} = K_n[2(V_{GS} - V_{TN})] = K_n 2\, V_{OV}$$

$$r_{DS} = \frac{1}{K_n 2\, V_{OV}}$$

$$= \frac{1}{[\mathrm{K_n}' \frac{\mathrm{W}}{\mathrm{L}} \mathrm{V_{OV}}]}$$

$$r_{DS} = \frac{1}{100 \times 10^{-6} \times 10 \times 0.5} = 20\mathrm{k}\Omega$$

2. For a $0.5\mu m$ process technology, for which $t_{ox} = 15\, nm$ & $\mu_n = 550\, {cm^2}/{_S}$. Find C_{ox}, $\mathrm{K_n}'$ and over drive voltage $V_{OV} = V_{GS} - V_{tN}$ required to operate a transistor having $\frac{\mathrm{W}}{\mathrm{L}} = 20$ in saturation region with $I_D = 0.2mA$. What the minimum value is of V_{DS}required?

Solution:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$\epsilon_{ox} = 3.9\epsilon_o = 3.9 \times 8.85 \times 10^{-14}$$

$$C_{ox} = \frac{3.45 \times 10^{-11}}{15 \times 10^{-9}} = 2.3\, {fF}/{\mu m^2}$$

$$K_n' = \mu_n C_{ox} = 127\,{}^{\mu A}/_{V^2}$$

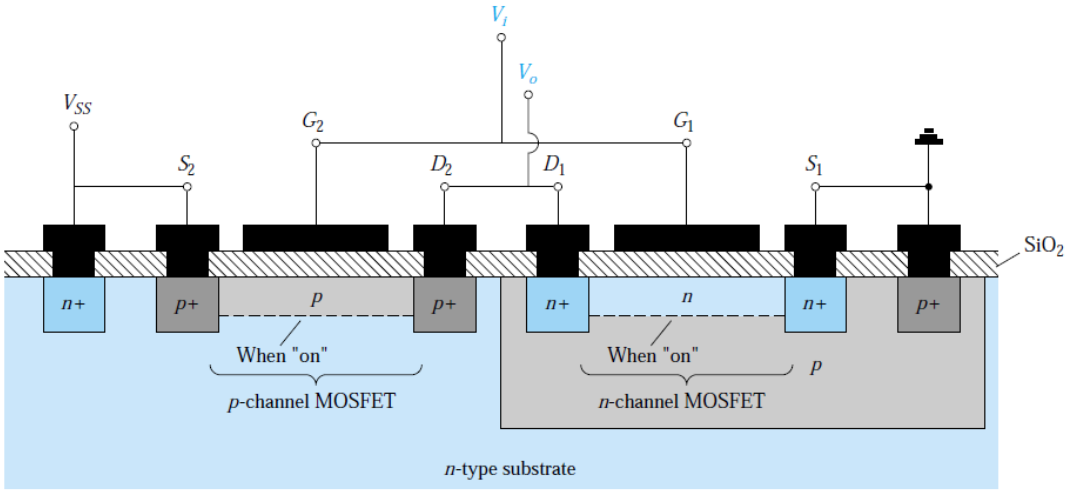
$$I_D = K_n(V_{GS} - V_{TN})^2$$

$$K_n = \frac{K_n' W}{2L} = 1270\,{}^{\mu A}/_{V^2}$$

$$V_{OV} \equiv V_{GS} - V_{tN} = \sqrt{\frac{I_D}{K_n}} = \sqrt{\frac{0.2 \times 10^{-3}}{1270 \times 10^{-6}}} = 0.4V$$

Complimentary MOS

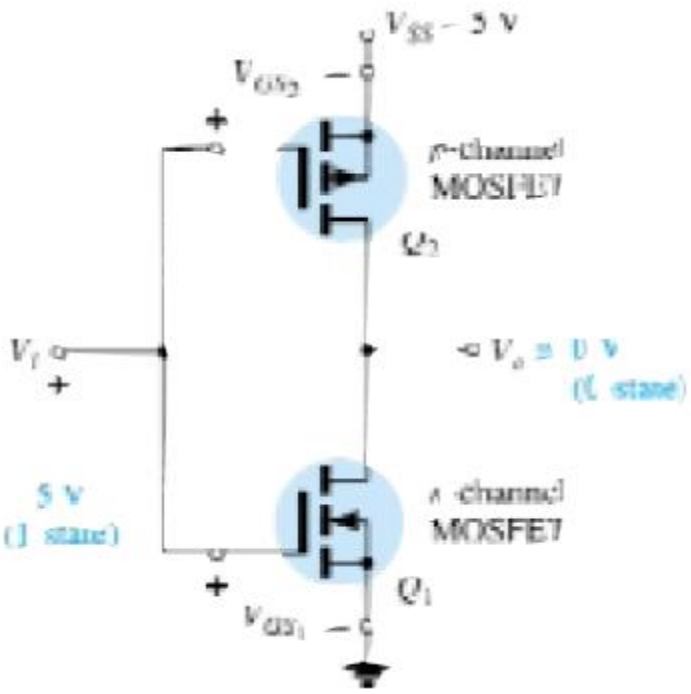
- ✓ A very effective logic circuit can be established by constructing a p-channel and an n-channel MOSFET on the same substrate as shown in Fig.
- ✓ The induced p-channel on the left and the induced *n*-channel on the right for the p- and n-channel devices, respectively.
- ✓ The configuration is referred to as a complementary MOSFET arrangement (CMOS) that has extensive applications in computer logic design.
- ✓ The relatively high input impedance, fast switching speeds, and lower operating power levels of the CMOS configuration have resulted in a whole new discipline referred to as CMOS logic design.



- ✓ One very effective use of the complementary arrangement is as an inverter, as shown in Fig.

- ✓ As introduced for switching transistors, an inverter is a logic element that “inverts” the applied signal.

- ✓ That is, if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level of 5 V, and vice versa.



- ✓ Both the gates are connected to the applied signal and both drain to the outputV_0.
- ✓ The source of the p-channel MOSFET (Q_2) is connected directly to the applied voltageV_{SS}, while the source of the *n*-channel MOSFET (Q_1) is connected to ground.

THE MOSFET AS AN AMPLIFIER AND AS A SWITCH

The basis for this important MOSFET application is that when operated in the saturation region, the MOSFET acts as a voltage-controlled current source: Changes in the gate-to-source voltage V_{GS} gives rise to drain current I_D. Thus the saturated MOSFET used to implement a transconductance amplifier. However, since we are interested in linear amplification—that is, in amplifiers whose output signal (in this case, the drain currentI_D) is linearly related to their input signal (in this case, the gate-to-source voltageV_{GS})—we will have to find a way around the highly nonlinear (square-law) relationship ofI_D toV_{GS}.

The technique we will utilize to obtain linear amplification from a fundamentally nonlinear device is that of **dc biasing** the MOSFET to operate at a certain appropriate $V_{GS}$and a correspondingI_D) and then superimposing the voltage signal to be amplified, V_{GS}, on the dc bias voltage V_{GS}. By keeping the signal v_{gs}"small," the resulting change in drain current, i_d), can be

made proportional tov_{gs}. We will study the total or large-signal operation of a MOSFET amplifier. We will do this by deriving the voltage transfer characteristic of a commonly used MOSFET amplifier circuit. From the voltage transfer characteristic we will be able to clearly see the region over which the transistor can be biased to operate as a small-signal amplifier as well as those regions where it can be operated as a switch (i.e., being either fully "on" or fully "off"). MOS switches find application in both analogue and digital circuits.

Large-Signal Operation-The Transfer Characteristic

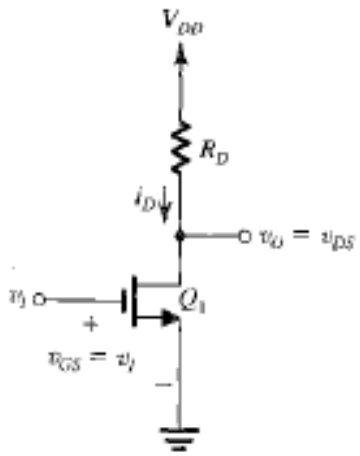


Figure shows the basic structure (skeleton) of the most commonly used MOSFET amplifier, the **common-source (CS)** circuit. The name common-source or **grounded-source** circuit arises because when the circuit is viewed as a two-port network, the grounded source terminal is common to both the input port, between gate and source, and the output port, between drain and source. Note that although the basic control action of the MOSFET is that changes in v_I as $v_{GS} = v_I$ give rise to changes ini_D**,** we are using a resistor R_D to obtain an output voltage v_0

$$v_0 = v_{DS} = v_{DD} - i_D R_D$$

In this way the transconductance amplifier is converted into a voltage amplifier. Finally, note that of course a dc power supply is needed to turn the MOSFET on and to supply the necessary power for its operation.

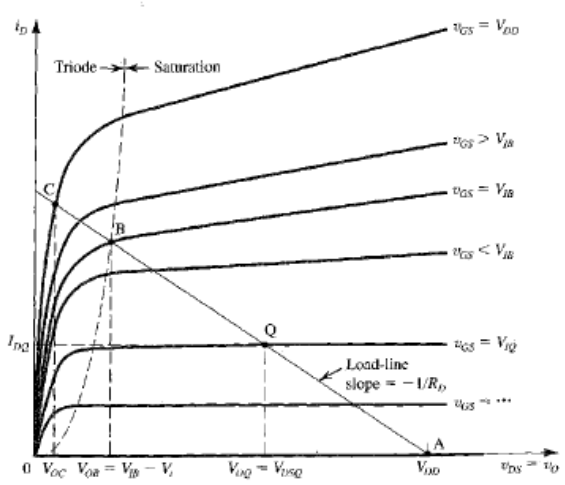
Graphical Derivation of the Transfer Characteristic

The operation of the common-source circuit is governed by the MOSFETs $i_D \sim v_{DS}$characteristics and by the relationship between $i_D and\ v_{DS}$imposed by connecting the drain to the power supply V_{DD} via resistorR_D, namely

$$v_{DS} = v_{DD} - i_D R_D$$

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS}$$

Figure shows a sketch of the MOSFETs $i_D \sim v_{DS}$ characteristic curves superimposed on which is a straight line representing the $i_D \sim v_{DS}$ relationship of Eq. Observe that the straight line intersects the v_{DS}-axis at V_{DD} [since from Eq. $v_{DS} = V_{DD}$ at$i_D = 0$] and has a slope of$-{}^{1}/_{R_D}$. Since R_D is usually thought of as the **load resistor** of the amplifier (i.e., the resistor across which the amplifier provides its output voltage), the straight line in Fig. is known as the **load line.**



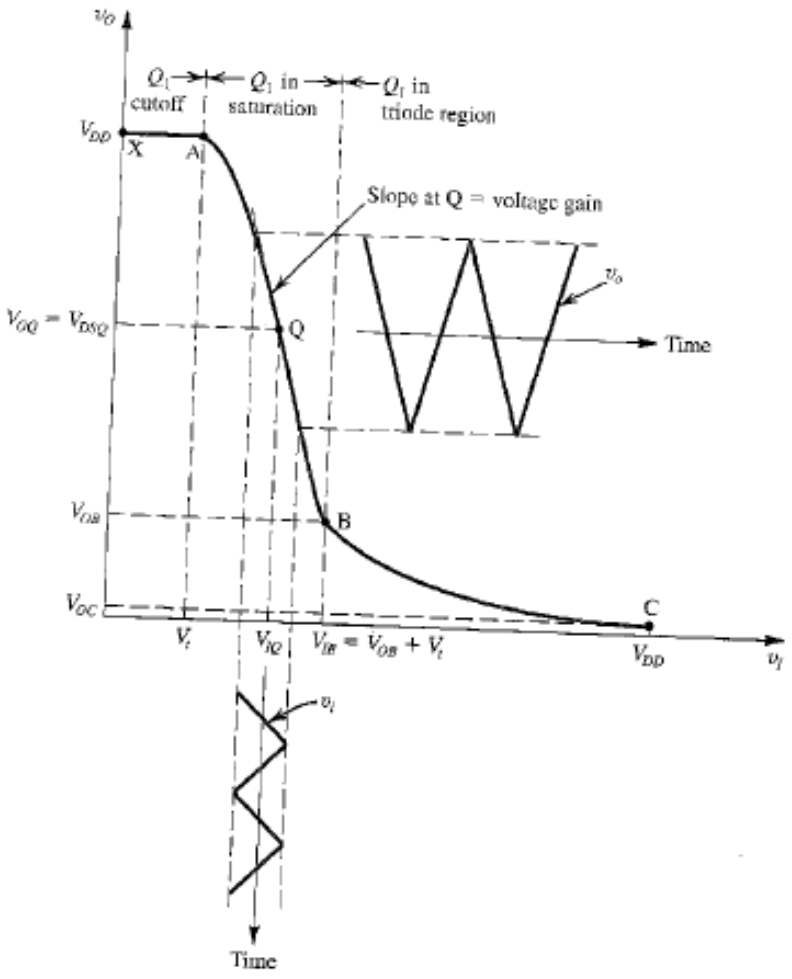
The graphical construction of Fig. can now be used to determine v_0(equal tov_{DS}) for each given value ofv_I ($v_{GS} = v_I$). Specifically, for any given value ofv_I. , we locate the corresponding $i_D \sim v_{DS}$ curve and find v_0 from the point of intersection of this curve with the load line.

Qualitatively, the circuit works as follows: Since $v_{GS} = v_I$ we see that for$v_I < V_t$, the transistor will be cut off, $i_D$will be zero, and$v_0 = v_{DS} = v_{DD}$. Operation will be at the point labelled A. As v_I exceedsV_t, the transistor turns on, i_D increases, and$v_0$decreases. Since$v_0$will initially be high, the transistor will be operating in the saturation region. This corresponds to points along the segment of the load line from A to B. We have identified a particular point in this region of operation and labelled it Q. It is obtained for $v_{GS} = v_{IQ}$and has the coordinates and$v_{OQ} = v_{DSQ} and\ i_{DQ}$

Saturation-region operation continues until v_0 decreases to the point that it is below v_I

by V_t , volts. At this point$v_{DS} = v_{GS} - V_t$, and the MOSFET enters its triode region of operation. This is indicated in Fig. by point B, which is at the intersection of the load line and the broken-line curve that defines the boundary between the saturation and the triode regions.

For$v_I > V_t$, the transistor is driven deeper into the triode region. Note that because the characteristic curves in the triode region are bunched together, the output voltage decreases slowly towards zero. Here we have identified a particular operating point C obtained for$v_I = v_{DD}$. The corresponding output voltageV_{OC}will usually be very small. This point-by point determination of the transfer characteristic results in the transfer curve shown in Fig. Observe that we have delineated its three distinct segments, each corresponding to one of the three regions of operation of MOSFETQ_1.



Operation as a Switch

When the MOSFET is used as a switch, it is operated at the extreme points of the transfer curve. Specifically, the device is turned off by keeping$v_I < V_t$, resulting$v_0 = V_{DD}$. The switch is turned on by applying a voltage closer toV_{DD}. Indeed, the common-source MOS circuit can be used as a logic inverter with the "low" voltage level close to 0 V and the "high" level close toV_{DD}.

Unit 3

Biasing of FETs and MOSFETs

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References: 1. "Electronic Devices and Circuit Theory"

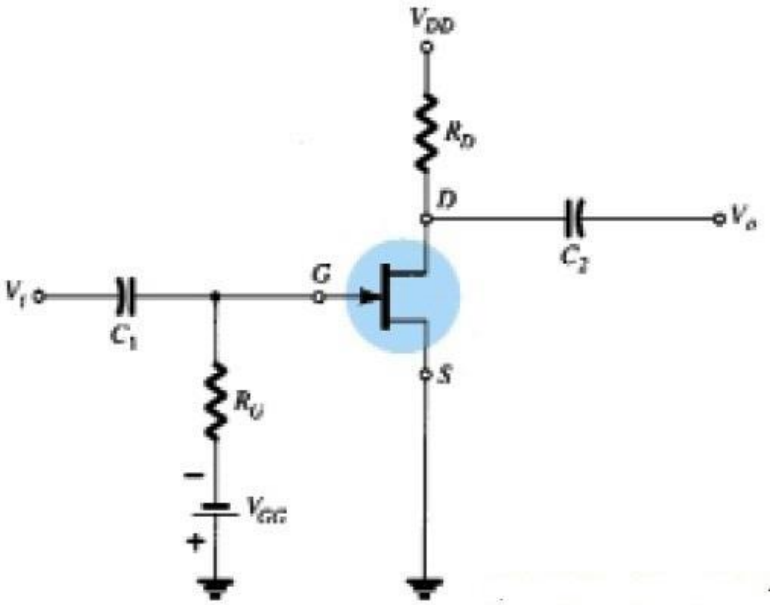
Robert L. Boylestad and L. Nashelsky

2. "Electronic Devices and Circuits"

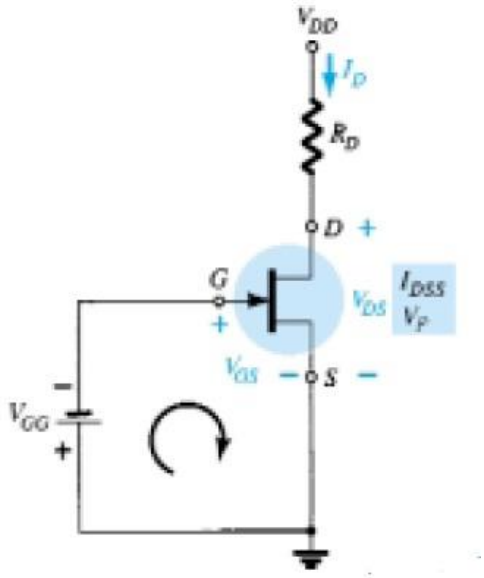
J.B. Gupta

FET biasing

Fixed bias Configuration



- ✓ Dc bias of a FET device needs setting of V_{GS} to give desiredI_D.
- ✓ For a JFET, drain current is limited by the saturation currentI_{DSS}.
- ✓ Since the JFET has such a high input impedance that no gate current flows and the dc voltage of the gate set by a fixed battery voltage.
- ✓ Fixed dc bias is obtained using a batteryV_{GG}. This battery ensures that the gate is always negative w.r.t. the source and no current flows through the resistor R_G and gate terminal i.e. $I_G = 0$. The battery provides a voltage V_{GS} to bias the n-channel JFET, but no resulting current is drawn from the batteryV_{GG}. The dc voltage drop across R_G is equal to $I_G R_G$ i.e. 0 volt.



- ✓ The gate-source voltage V_{GS} is then

$$V_{GS} = V_G - V_S = -V_{GG}$$

- ✓ The gate-source current I_D is then fixed by the gate-source voltage as determined by the equation

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

- ✓ This current then causes a voltage drop across the drain resistor R_D and is given by

$$V_{RD} = I_D R_D$$

And the output voltage

$$V_0 = V_{DD} - I_D R_D$$

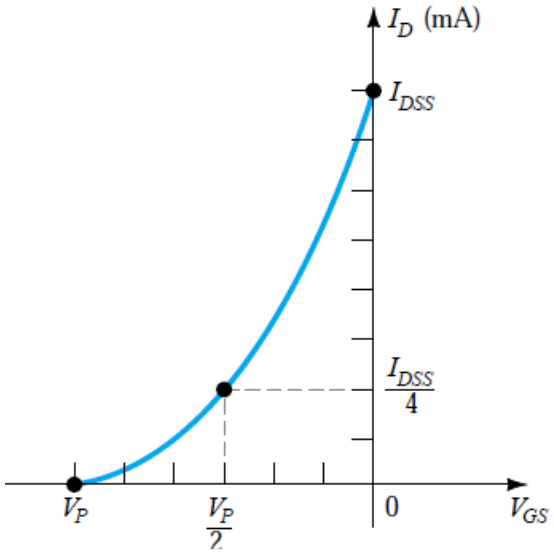
- ✓ Since V_{GG} is fixed value of dc supply and the magnitude of V_{GS} is also fixed, hence the circuit is named as fixed-bias circuit.

- ✓ Since this bias circuit uses two batteries V_{GG} and V_{DD}, it is also known as two battery bias circuit.

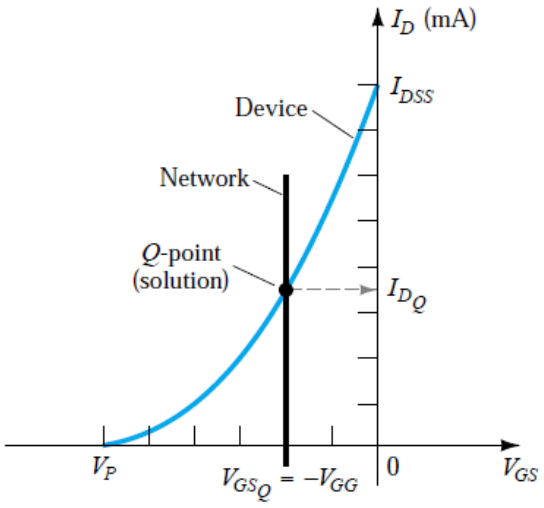
- ✓ A FET has high input impedance. To make advantage of it, R_G should be as large as possible so that input impedance of the circuit remains high. A reasonable upper limit is 1MΩ. Normally R_G should not exceed this value.

Graphical Analysis

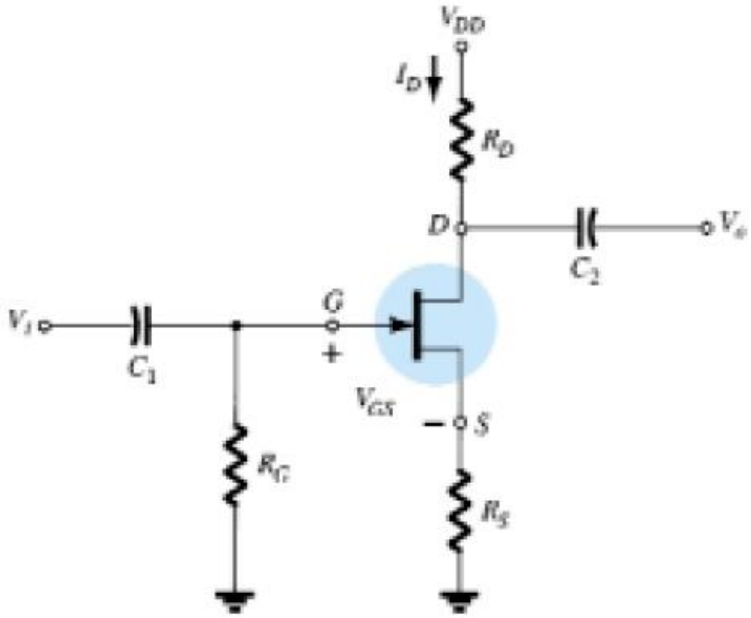
A graphical analysis would require a plot of Shockley's equation as shown in Fig. By choosing $V_{GS} = V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis, the three points defined by I_{DSS} , V_P and the intersection just described will be sufficient for plotting the curve.



In Fig., the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$-the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration-commonly referred to as the quiescent or operating point. The subscript Q will be applied to drain current and gate-to-source voltage to identify their levels at the Q-point. Note in Fig. that the quiescent level of I_D is determined by drawing a horizontal line from the Q-point to the vertical I_D axis as shown in Fig.



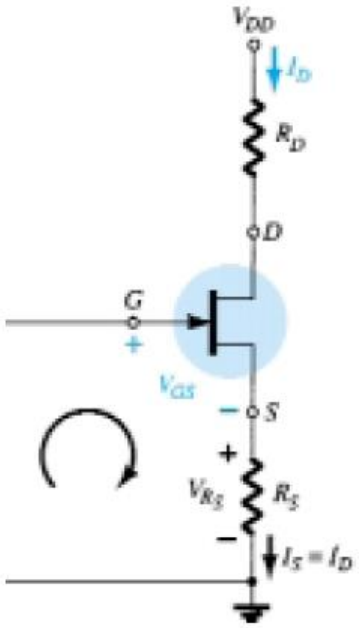
Self bias Configuration



- ✓ This is the most common method of biasing a JFET.

- ✓ This circuit eliminates the requirement of two dc supplies i.e. only drain supply is used and no gate supply is connected.

- ✓ In this circuit, a resistorR_S, known as bias resistor, is connected in the source lag.
  The dc component of drain current I_D flowing through R_S makes a voltage drop acrossR_S.
  The voltage drop across R_S reduces the gate-to-source reverse voltage required for JFET operation. The resistorR_S, feedback resistor prevents any variation in drain current.



- ✓ since no gate current flows through the reverse bias gate-source, the gate current $I_G = 0$ and therefore, $V_G = I_G R_G = 0V$

- ✓ with the drain current I_D the voltage at source

$$V_S = I_D R_S = 0V$$

  And the gate-source voltage V_{GS} is

$$\boxed{V_{GS} = V_G - V_S = -I_D R_S}$$

- ✓ So the voltage drop across the resistanceR_S, provides the biasing voltage V_{GS} and no external source is required for biasing, and this is the reason that it is called self biasing.

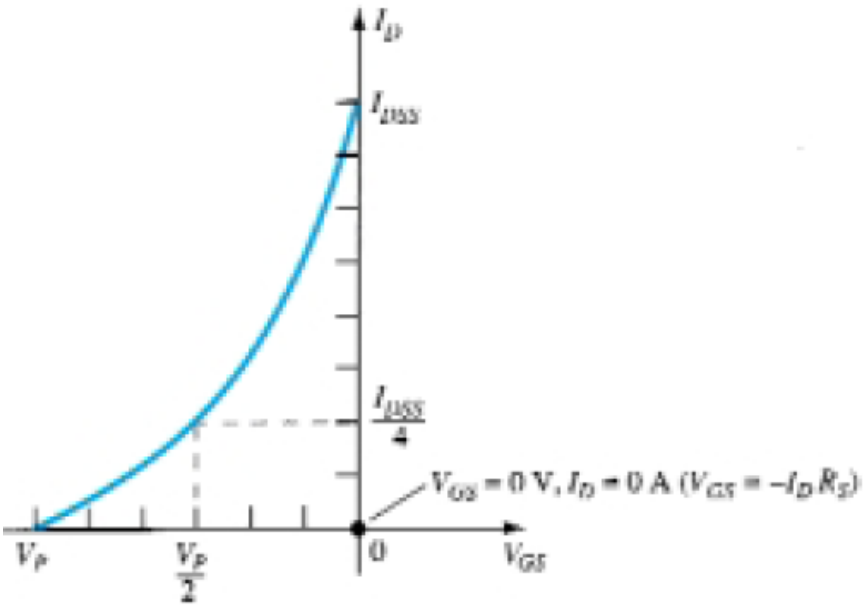
- ✓ The operating point (i.e. zero signal I_D and V_{DS}) can easily be determined by the equations

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Graphical Analysis

The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. Since Eq. $V_{GS} = -I_D R_S$ defines a straight line on the same graph, let us now identify two points on the graph that are on the line and simply draw a straight line between the two points. The most obvious condition to apply is $I_D = 0A$ since it results in $V_{GS} = -I_D R_S = 0V$. For Eq., therefore, one point on the straight line is defined by$I_D = 0A and\, V_{GS} = 0V$, as appearing on Fig.

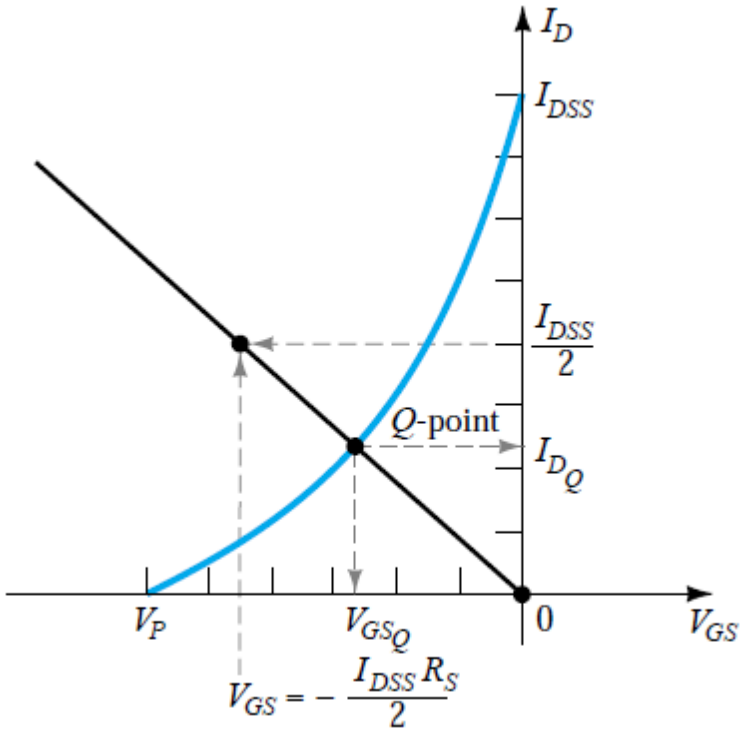


The second point for Eq. requires that a level of $V_{GS}\ or\ I_D$ be chosen and the corresponding level of the other quantity be determined using Eq. The resulting levels of $V_{GS}\ and\ I_D$will then define another point on the straight line and permit an actual drawing of the straight line. Suppose, for example, that we choose a level of $I_D$equal to one-half the saturation level. That is,

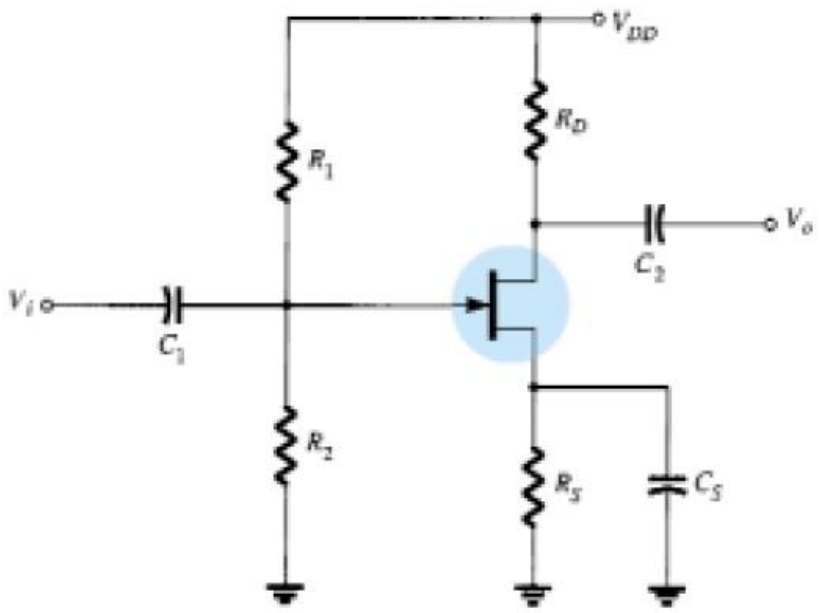
$$I_D = \frac{I_{DSS}}{2}$$

$$V_{GS} = -I_D R_S = -\frac{I_{DSS}}{2} R_S$$

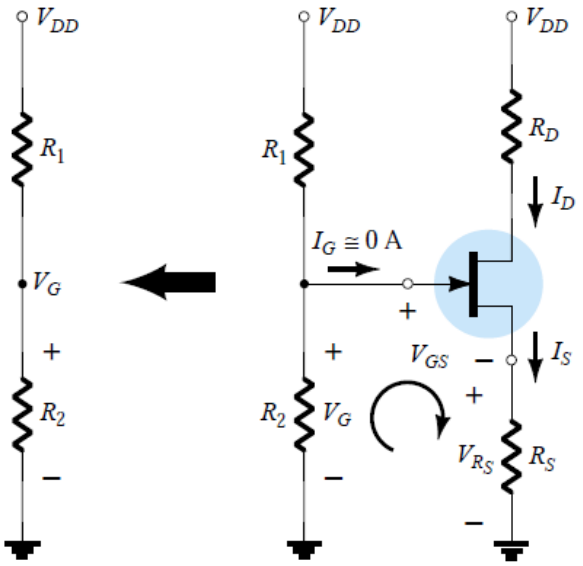
The result is a second point for the straight-line plot as shown in Fig. The straight line as defined by Eq. is then drawn and the quiescent point obtained at the intersection of the straight-line plot and the device characteristic curve. The quiescent values of V_{GS} *and* I_D can then be determined and used to find the other quantities of interest.



Voltage-divider bias Configuration



- ✓ The resistor R_1 and R_2 form a potential divider across the drain supplyV_{DD}.
- ✓ The voltage V_2 across R_2 provides necessary bias. The additional gate resistor R_1 form gate to supply voltage facilitates in larger adjustment of the dc bias point and permits use of large valuedR_S.



- ✓ The gate is reverse biased so that $I_G = 0$ and the gate voltage

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} R_2$$

And

$$\boxed{V_{GS} = V_G - I_D R_S}$$

- ✓ The circuit is so designed so that $I_D R_S$ is larger than V_G so that V_{GS} is negative. This provides correct bias voltage.

- ✓ The operating point can be determined as

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$$

- ✓ Maximum gain is achieved by making resistance R_D as large as possible and for a given level of I_D it needs maximum voltage drop across resistor R_D. However, greater bias stability is achieved by making R_S as large as possible.

Graphical Analysis

$$\boxed{V_{GS} = V_G - I_D R_S}$$

Since any straight line requires two points to be defined, let us first use the fact that anywhere on the horizontal axis of Fig. the current $I_D = 0$. If we therefore select I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0mA$ into Eq. and finding the resulting value of V_{GS} as follows:

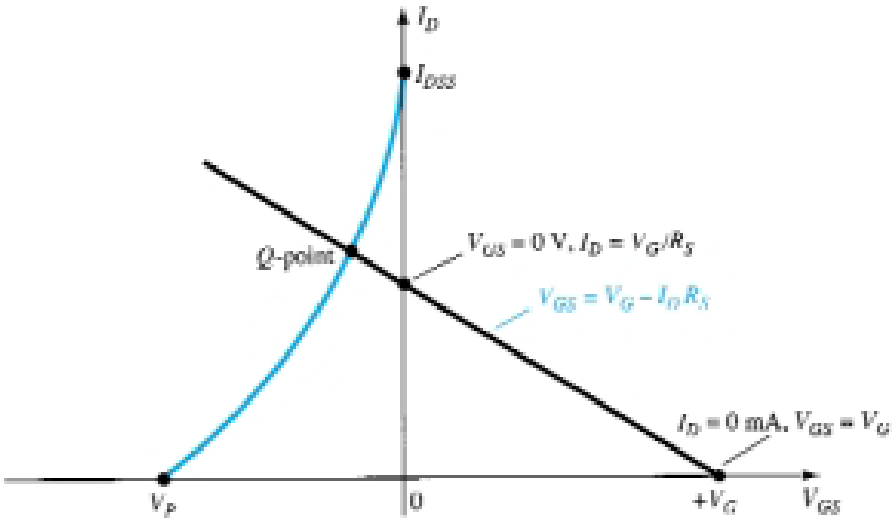
$$V_{GS} = V_G$$

The result specifies that whenever we plot Eq., if we choose $I_D = 0mA$, the value of for the plot V_{GS} will be V_G volts. The point just determined appears in Fig.

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0V$ and solve for the resulting value of I_D:

$$I_D = \frac{V_G}{R_S}$$

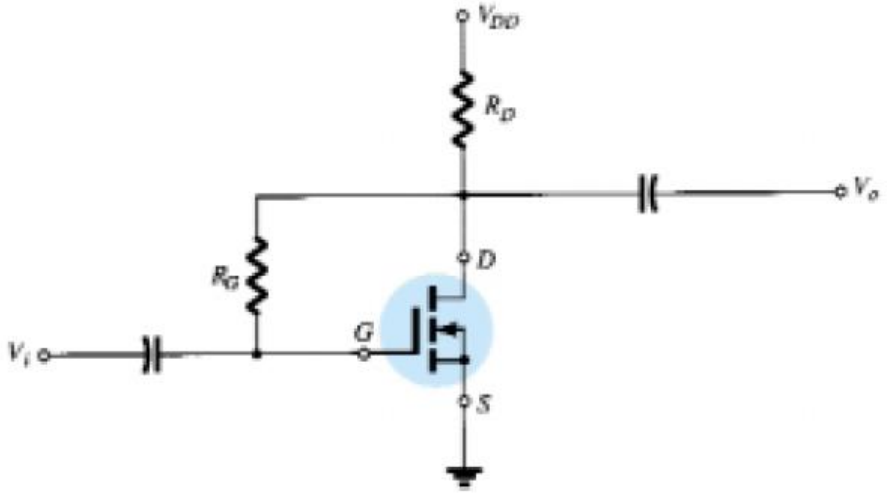
The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of I_D and V_{GS}.



Biasing of MOSFETs

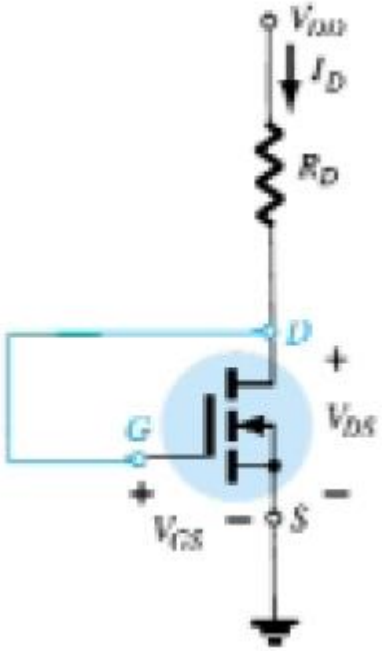
Feedback Biasing Arrangement

- ✓ A popular biasing arrangement for enhancement-type MOSFETs is provided in Figure.



- ✓ The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on."

- ✓ Since $I_G = 0mA$ and $V_{R_G} = 0V$, the dc equivalent network appears as shown in Fig.



- ✓ A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

$$V_{DS} = V_{GS}$$

- ✓ For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

which becomes

$$V_{GS} = V_{DD} - I_D R_D$$

- ✓ Since the Eq. is that of a straight line, the procedure employed to determine the two points that will define the plot on the graph is as follows:
  Substituting $I_D = 0mA$ into Eq. gives

$$V_{GS} = V_{DD} | I_D = 0mA$$

  Substituting $V_{GS} = 0V$ into Eq.

$$I_D = \frac{V_{DD}}{R_D} \Big| V_{GS} = 0V$$

- ✓ The plots defined by the above Eqs. appear in Fig. with the resulting operating point.