Module-IV

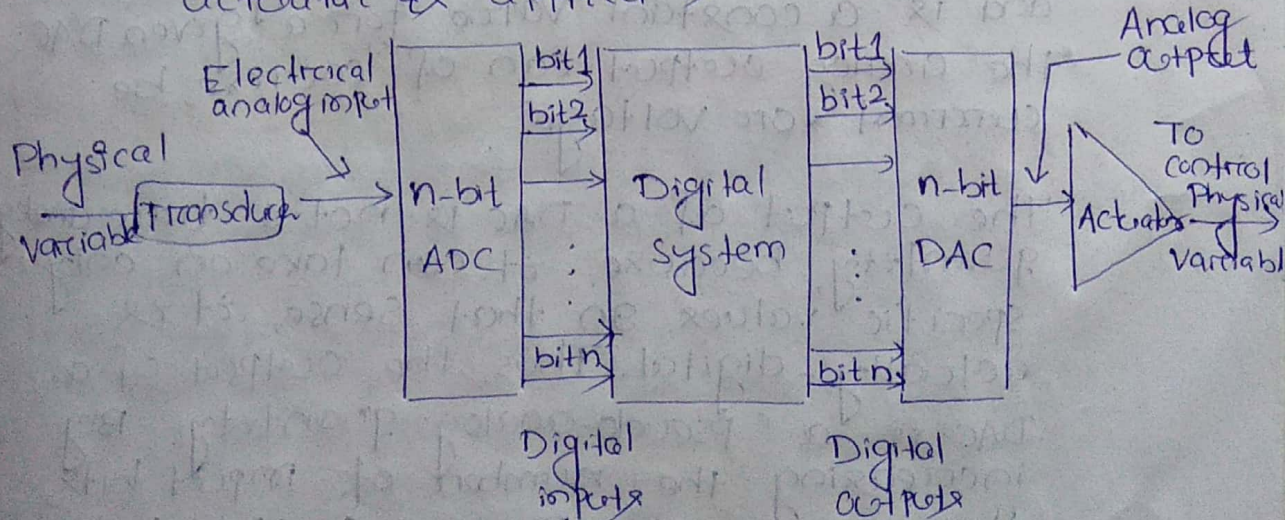
A/D and D/A converters

Introduction

An analog quantity is one that take on any value over a continuous range of values. It represents an exact value. Most physical variables are analog in nature. Temperature, pressure, Light and sound intensity, position, rotation, speed etc. are some examples of analog quantities.

A digital quantity takes on only discrete values. The value is expressed in a digital code such as a binary or BCD number.

When a physical process is monitored or controlled by a digital system such as a digital computer, the physical variables are first converted into electrical signals using transducers, then these electrical analog signals are converted into digital signals using analog to digital converters (ADCs). These digital signals are processed by a digital computer and the output of the digital computer is converted into analog signals using digital-to-analog converters (DACs). The output of the DAC is modified by an actuator and the output of actuator is applied as a control variable.



Interfacing a digital computer to the analog world

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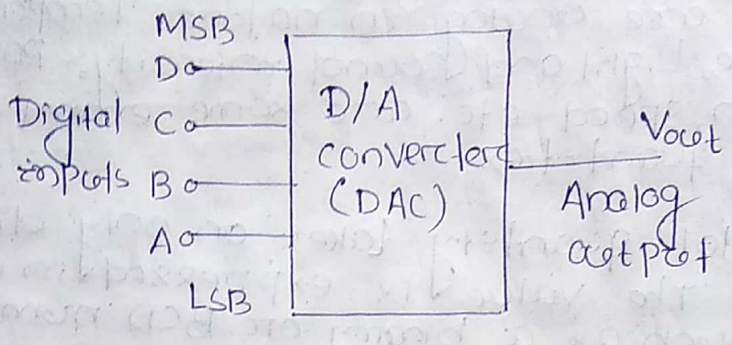
Digital-to-Analog (D/A) conversion

Basically, D/A conversion is the process of converting a value represented in digital code, such as straight binary or BCD, into a voltage or current which is proportional to the digital value.



Block diagram of a 4-bit DAC

Each of the digital inputs A, B, C, and D can assume a value of 0 or a 1, therefore there are $2^4 = 16$ possible combinations of inputs. For each input number 0000, 0001, ... 1111, the D/A converter outputs a unique value of voltage. The analog output voltage Vout is proportional to the input binary number i.e.

$$\text{Analog output} = K \times \text{digital input}$$

where K is the proportionality factor and is a constant value for a given DAC. The analog output can of course, be current or voltage.

The output of a DAC is not a true analog quantity, because it can take on only specific values. In that sense, it is actually digital. Thus, the output of a DAC is a 'pseudo-analog quantity. By increasing the number of input bits, the number of possible output values can be increased and also the step size (the difference between two successive output values) can be reduced, thereby producing an output that is more like an

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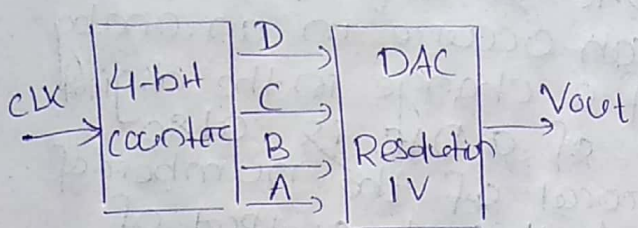
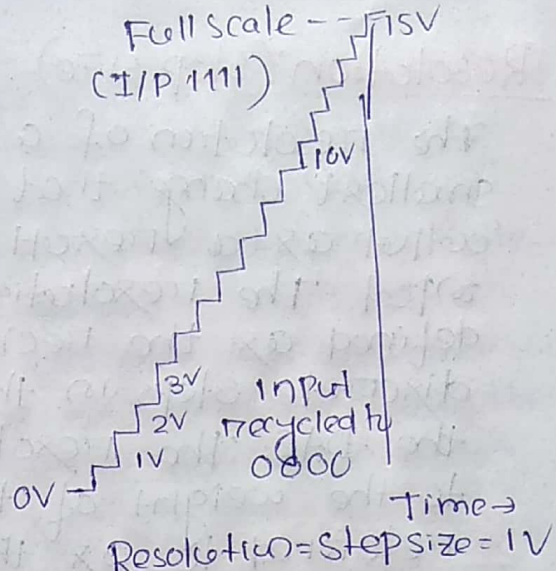
analog quantity.





Output waveform of a DAC fed by a binary counter

When the binary counter is continually recycled through its 16 states by applying the clock signal, the DAC output will be a staircase waveform with a step size of 1V. When the counter is at 0000, the output of DAC is minimum (0V). When the counter is at 1111, the output of DAC is maximum (15V). This is the full-scale output.

Digital-to-analog and analog-to-digital conversion form the very important aspects of digital data processing. Digital-to-analog conversion is a straightforward process and is considerably easier than the A/D conversion. In fact, a DAC is usually an integral part of any ADC.

Specification for D/A converters

The characteristics of a D/A converter, which is generally specified by the manufacturers, are

1. Resolution
2. Accuracy
3. Settling time
4. Offset voltage
5. Temperature sensitivity

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Resolution (Step Size)

The resolution of a DAC is defined as the smallest change that can occure in an analog output as a result of a change in the digital input. The resolution of a DAC is also defined as the reciprocal of the number of discrete steps in the full-scale output of the DAC. The resolution is always equal to the weight of the LSB and is also referred to as the step size.

The resolution or step size is the size of the jumps in the staircase waveform.

Although resolution can be expressed as the amount of voltage or current per step, it is also useful to express it as a percentage of the full-scale output.

$$\%\text{ resolution} = \frac{\text{step size}}{\text{full scale}} \times 100\%$$

Since, full scale = number of steps × step size, resolution can be expressed as

$$\%\text{ resolution} = \frac{1}{\text{total number of steps}} \times 100\%$$

In general, for an N-bit DAC, the number of different levels will be 2^N, and the number of steps will be $2^N - 1$. The greater the number of bits, the greater will be the number of steps and smaller will be the step size and therefore, the finer will be the resolution. Of course, the cost of DAC increases with the number of input bits.

Alternatively, the number of bits accepted at the input can itself be used as the resolution. For example, an 8-bit D/A converter has an 8-bit resolution.

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Accuracy

The accuracy of a D/A converter is a measure of the difference between the actual output voltage and the expected output voltage. It is specified as a percentage of full scale or maximum output voltage.

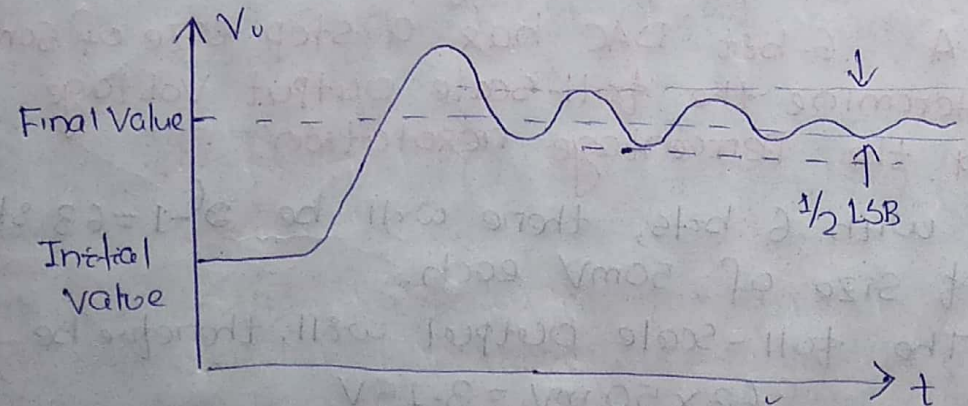
For example, if a D/A converter has 10V full-scale output voltage and an accuracy of ±0.2%, then the maximum error for any output voltage will be $0.002 \times 10 = 20mV$

Settling time

The operating speed of a DAC is usually specified by its settling time. When the digital input to a D/A converter changes, the analog output voltage does not change abruptly. Because of the presence of switches, active devices, stray capacitance and inductance associated with the passive circuit components, the transients appear in the output voltage and oscillations may also occur.

It is defined as the total time between the instant when the digital input changes and the time that the output enters & specified error band for the last time, usually ±1/2 LSB around the final value after the change in digital input.

It is measured as the time for the DAC output to settle within ±1/2 step size of its final value.



Settling time of a D/A Converter

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Offset Voltage

Ideally, the output of a DAC should be zero when the binary input is zero. In practice, however, there is a very small output voltage under this situation called the offset voltage. This offset error, if not corrected, will be added to the expected DAC output for ALL input cases.

Temperature Sensitivity

The analog output voltage for any fixed digital input varies with temperature. This is due to the temperature sensitivities of the reference voltage source, resistors, OPAMP etc. It is specified as ± PPM/°C.

Ex Determine the resolution of (a) a 6-bit DAC and that of (b) a 12-bit DAC in terms of percentage.

a) For the 6-bit DAC,

$$\% \text{ resolution} = \frac{1}{2^N - 1} \times 100 = \frac{1}{2^6 - 1} \times 100$$

$$= \frac{1}{63} \times 100 = 1.587\%$$

b) For 12-bit DAC,

$$\% \text{ resolution} = \frac{1}{2^N - 1} \times 100 = \frac{1}{2^{12} - 1} \times 100$$

$$= 0.0244\%$$

Ex A 6-bit DAC has a step size of 50mV. Determine the full-scale output voltage and the percentage resolution.

With 6 bits, there will be $2^6 - 1 = 63$ steps of size of 50mV each.

The full-scale output will, therefore be

$$63 \times 50 \text{ mV} = 3.15 \text{ V}$$

$$\% \text{ resolution} = \frac{1}{2^N - 1} \times 100 = \frac{1}{2^6 - 1} \times 100 = 1.587\%$$

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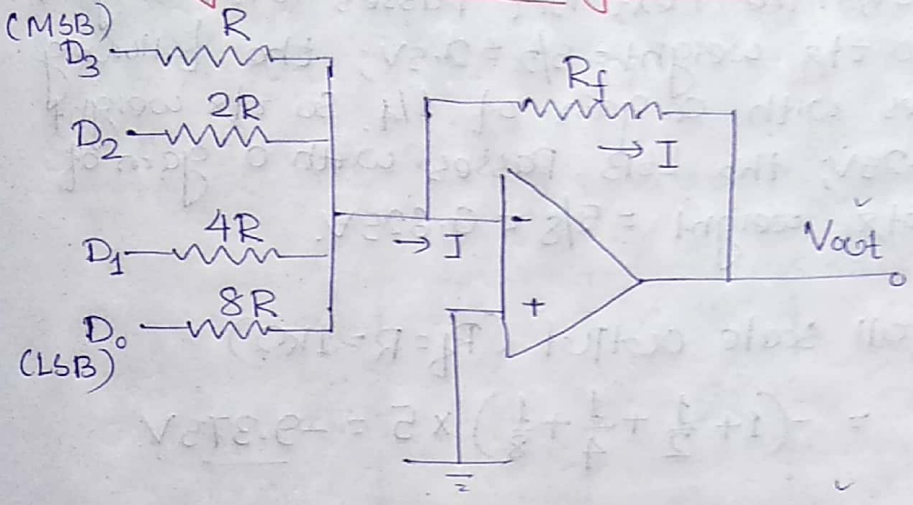
OR, % resolution = $\frac{\text{step size}}{\text{full scale}} \times 100$

$= \frac{50mV}{3.15V} \times 100 = 1.587\%$

* Full-scale output = Step size x Number of steps $(2^N - 1)$

The Weighted-Resistor type DAC



Weighted resistor type DAC

The operational amplifier is used to produce a weighted sum of the digital inputs, where the weights are proportional to the weights of the bit positions of inputs. Since the opamp is connected as an inverting amplifier, each input is amplified by a factor equal to the ratio of the feedback resistance divided by the input resistance to which it is connected. The MSB D_3 is amplified by R_f/R, D_2 is amplified by $R_f/2R$, D_1 is amplified by $R_f/4R$, and D_0, the LSB is amplified by $R_f/8R$.

The inverting terminal of the op-amp acts as a virtual ground.

$$V_{out} = -\left(D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8}\right) \times \left(\frac{R_f}{R}\right)$$

The main disadvantage of this type of DAC is that a different-valued precision resistor must be used for each bit position of the digital input.

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Ex For the 4-bit weighted resistor DAC determine a) the weight of each input bit if the inputs are 0V and 5V b) the full-scale output, if $R_f = R = 1k\Omega$. Also find the full-scale output if R_f is changed to 500Ω.

a) The MSB passes with a gain of 1, so its weight = 5V; the next bit passes with a gain of 1/2. So its weight = 5/2 = 2.5V; the following bit passes with a gain of 1/4. So its weight = 5/4 = 1.25V; the LSB passes with a gain of 1/8. So its weight = 5/8 = 0.625V.

b) the full scale output ($R_f = R = 1k\Omega$)

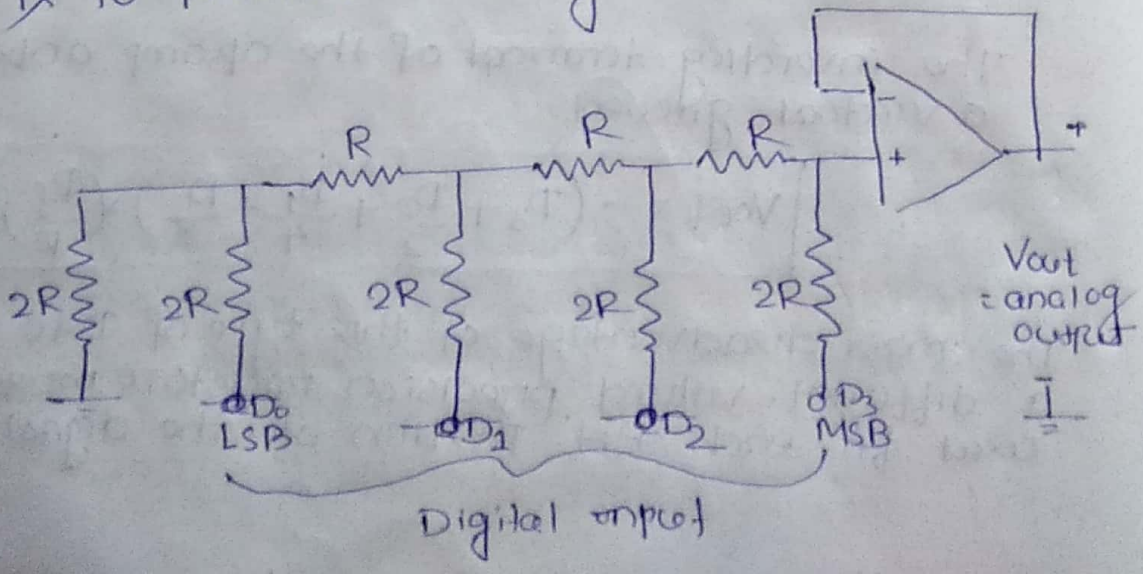
$$= -\left(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}\right) \times 5 = -9.375V$$

The full-scale output, when R_f is changed to 500Ω is

$$V_{out} = -\left(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}\right) \times \left(\frac{5}{2}\right) = -4.6875V$$

The R-2R Ladder type DAC

This is the most popular DAC. It uses a ladder network containing series-parallel combinations of two resistors of values R and 2R. Hence the name. The operational amplifier configured as voltage follower is to prevent loading.



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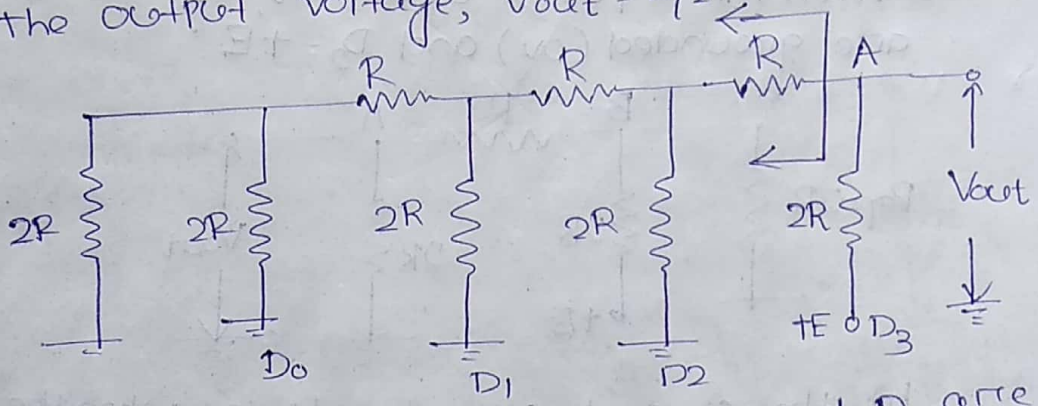
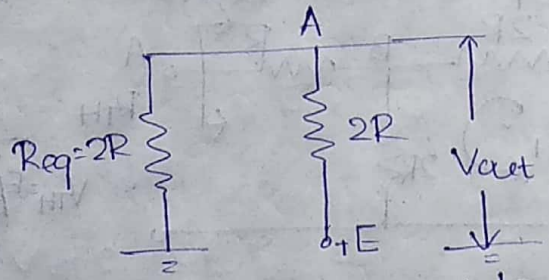
When a digital signal $D_3D_2D_1D_0$ is applied at the input terminals of the DAC, an equivalent analog signal is produced at the output terminal. The operation of the DAC is as follows

Case-1: When the input is 1000

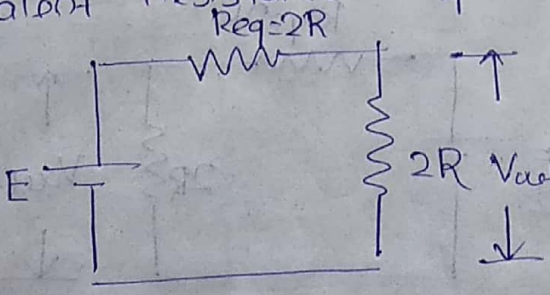
In the Left hand of the Ladder, 2R is in parallel with 2R, so that the equivalent combination is R. This R is in series with another R giving 2R. This 2R is parallel with another 2R is equivalent to R. continuing in this manner, we ultimately find that $R_{eq} = 2R$. the output voltage, $V_{out} = E/2$



a) When the input is 1000; D_0, D_1 and D_3 are grounded (0V) and $D_3 = +E$



b) The circuit equivalent to (a) when the circuit to the left of A is replaced by its equivalent resistance R_{eq}



c) calculation of V_{out} using voltage divider rule.

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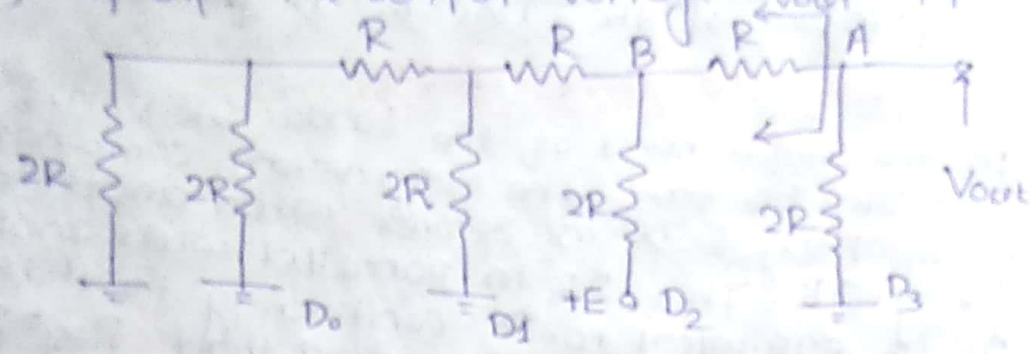
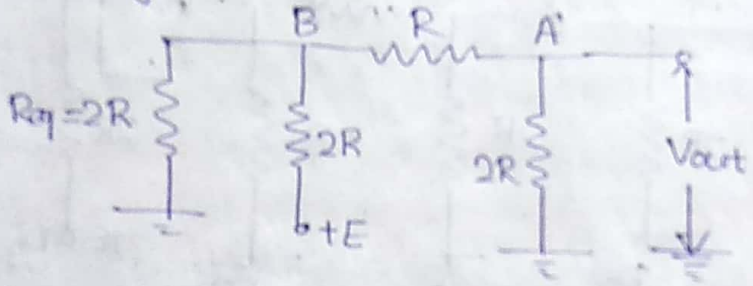
Case 2: When the input is 0100

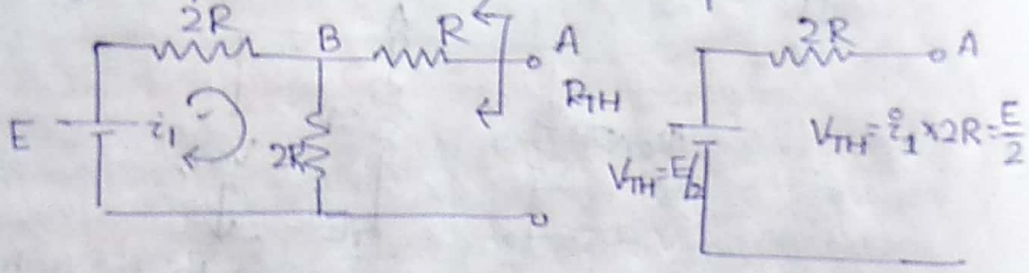
Here, we find that to the Left of terminal B, $R_{eq} = 2R$. The output voltage $V_{out} = E/4$.



a) When the input is 0100, D_0, D_1, and D_3 are grounded (0V) and $D_2 = +E$.

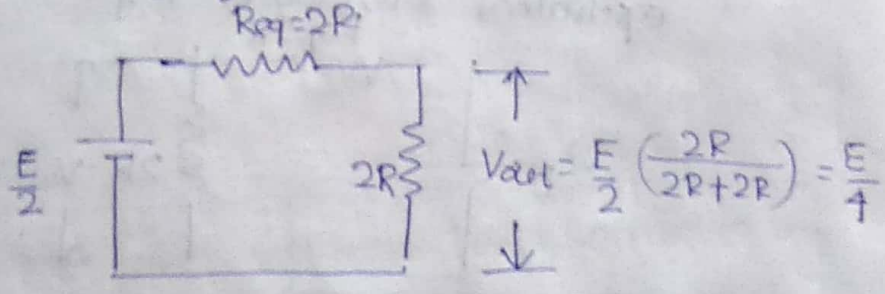


b) the circuit equivalent to (a) when the circuit to the Left of B is replaced by its equivalent resistance R_{eq}



c) Thevenin's equivalent to the left of A

$R_{TH} = [(2R \| 2R) + R] = 2R$



d) calculation of V_{out} using voltage divider rule.

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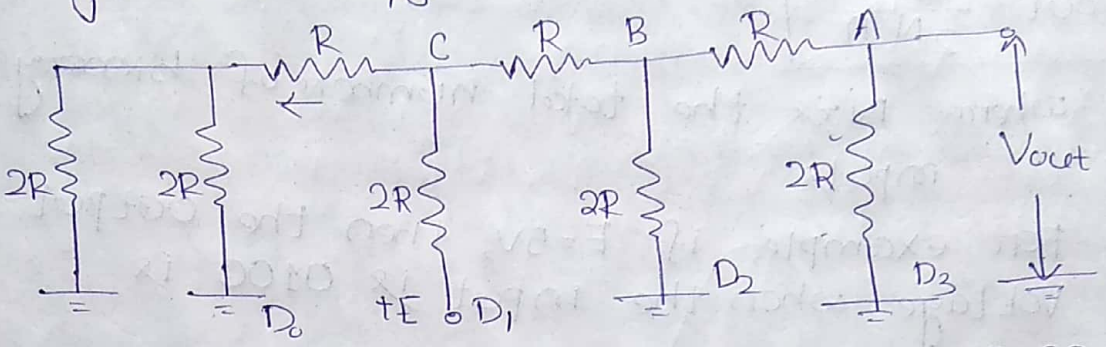
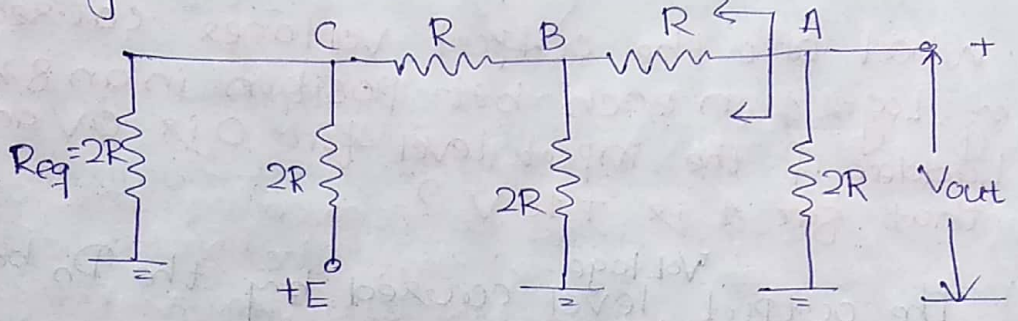
Case-3: When the input is 0010

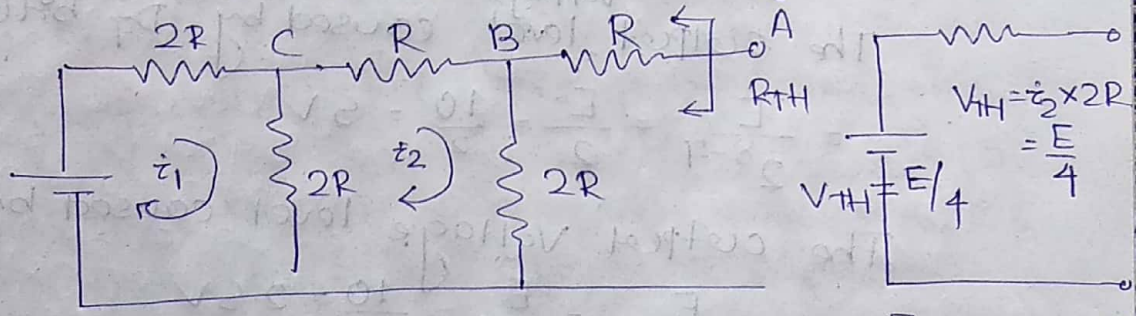
Here Req to the Left of C is 2R. The output voltage, $V_{out} = E/8$



a) When the input is 0010, D_0, D_2, & D_3 are grounded (0V) and $D_1 = +E$

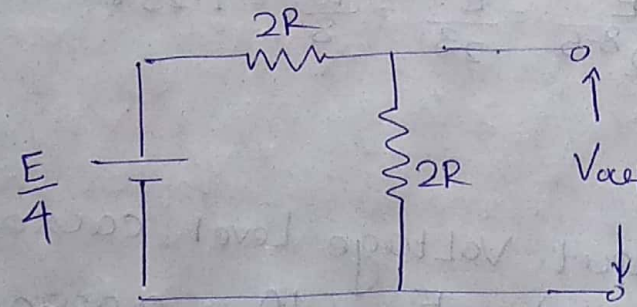


b) The circuit to a) when the circuit to the left of C is replaced by $R_{eq} = 2R$



c) Thevenin's equivalent to the Left of A

$R_{TH} = [(2R \| 2R) + R] \| 2R + R = 2R$



$V_{out} = \frac{E}{4}\left(\frac{2R}{2R+2R}\right) = \frac{E}{8}$

d) Calculation of V_{out} using the voltage divider rule

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In general, when D_n input is a 1, and all other inputs are a 0, the output is

$$V_{out} = \frac{E}{2^{N-n}}$$

where, N is the total number of binary inputs

For example, if E=5V, then the output voltage when the input is 0100 is

$$\frac{5}{2^{4-2}} = \frac{5}{4} = 1.25\,V$$

Ex What are the output voltages caused by Logic 1 in each bit position in an 8-bit Ladder if the input level for 0 is 0V and that for 1 is +10V?

The output voltage level caused by the D_0 bit is

$$\frac{E}{2^{N-n}}$$

The output voltage level caused by D_7 bit (MSB)

$$= \frac{E}{2^{8-7}} = \frac{E}{2} = \frac{10}{2} = 5V$$

The output voltage level caused by D_6 bit

$$= \frac{E}{2^{8-6}} = \frac{E}{2^2} = \frac{10}{4} = 2.5V$$

The output voltage level caused by D_5 bit

$$= \frac{E}{2^{8-5}} = \frac{E}{2^3} = \frac{10}{8} = 1.25V$$

The output voltage level caused by the D_0 bit (LSB) $= \frac{E}{28} = \frac{10}{256} = 0.03906V$

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Example of D/A converter IC

The AD DAC 80 is a 12-bit D/A converter, available in 24-Pin DIP. It consists of matched bipolar switches, a precision resistor network, a low drift, high-stability voltage reference with an optional output amplifier. The options available are 12-bit complementary binary (CBI) or three-digit BCD (complementary-coded decimal, CCD) input codes, as well as current or voltage output modes. Its important performance characteristics are:

Resolution	: 12 bit (binary) or 3 digits (BCD)
Linear error	: ±0.12% (max)
Maximum gain drift	: ±30 ppm/°C
Power dissipation	: 925 mW (max)
Maximum conversion time	: 5 μs (voltage output) 1 μs (current output)
Digital input format	: 12bit CBI or 3-digit CCD
Analog output voltage ranges	: ±2.5V, ±5V, ±10V, 0 to +5V
Output current	: ±5mA (min)
Output impedance (dc)	: 0.05Ω
Analog output current ranges	: ±1mA, 0 to -2mA (CBI) or 0 to -2mA (CCD)
Output impedance	: 3.2kΩ (bipolar) or 6.6kΩ (unipolar)

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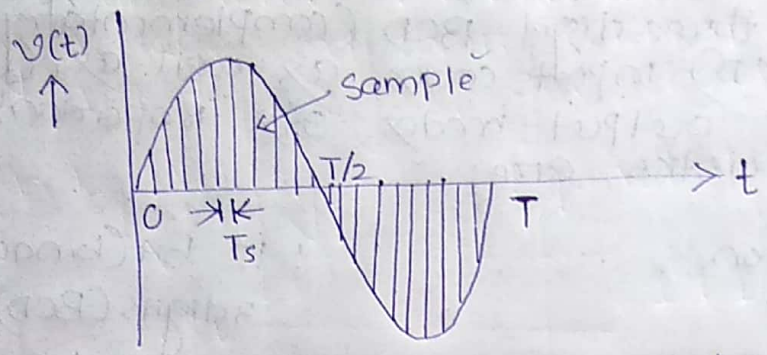
Sample and hold

A time-varying analog signal can have any value in a given range. For example, $v(t) = V\sin\omega t$ will have different value of voltage between the range $+V$ and $-V$ at different instants of time.



A time varying analog signal
$v(t) = V\sin\omega t$

If this signal is to be converted into digital form, we may think that the value of the signal at every instant of time is required to be converted into a group of n number of bits. This process will yield an infinite number of analog voltage values and thus is not at all practicable. On the other hand, if we take the samples of $v(t)$ at regular intervals, that is the signal is sampled regularly every T_s, then according to sampling theorem, the signal can be uniquely determined and reconstructed from these samples with no error. The time T_s is called the sampling time and $f_s = \frac{1}{T_s}$ is sampling rate.

According to the sampling theorem,

$$\boxed{f_s \geq 2f}$$

where f is the frequency of the analog signal.

The constant voltage corresponding to each sample is obtained using a sample-and-hold (S/H) circuit. The output of the S/H circuit is converted to digital signal by means of an analog-to-digital (A/D) converter circuit.

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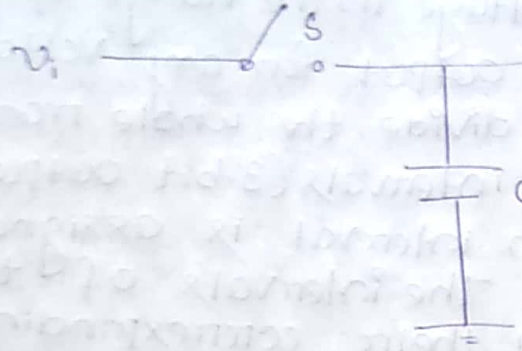
Sample-and-Hold Circuit



Basic sample-and-hold circuit

In this circuit the voltage across the capacitor follows the input signal v_i during the time switch S is closed. The capacitor holds the instantaneous value of the signal voltage attained just before the switch is opened. Thus for every T_s, the switch is closed for a short duration and then opened. The dc voltage across the capacitor gives the value of the signal at the instant the switch is opened. This dc voltage represents a sample of the signal and is converted to digital signal using A/D converter circuit during the hold period.

Analog-to-Digital Converters

Quantization & Encoding

In digital-to-analog converter, the possible number of digital inputs is fixed. For example, in a 3-bit D/A converter, there are 8 possible inputs. In contrast, in an analog-to-digital converter, the input analog voltage can have any value in a range, but the digital output can have only 2^N discrete values for an N-bit A/D converter. Therefore, the whole range of analog voltage is required to be represented suitably in 2^N intervals. This process is known as quantization. Each interval is then assigned a unique N-bit binary code, which is referred to as encoding.

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Consider an analog voltage in the range of 0 to V and a 3-bit digital output for any voltage in this range. Let us divide the whole range of analog voltage in 8 intervals (3-bit output) of the size S = V/8. Each interval is assigned a 3-bit binary value. The intervals of the analog voltage and their corresponding digital values assigned are shown

Analog Voltage	Equivalent digital value
V	
7/8V	111
6/8V	110
5/8V	101
4/8V	100
3/8V	011
2/8V	010
1/8V	001
0	000

From this, we observe that the whole range of voltage in an interval is represented by only one digital value. Therefore, there is an error referred to as quantization error, involved in this process of quantization.

In this case, the maximum quantization error for any analog input voltage Vs in the given range is V/8.

The quantization error can be reduced if we choose the middle six intervals of size S = V/7 and the top and the bottom intervals of size S/2 = V/14.

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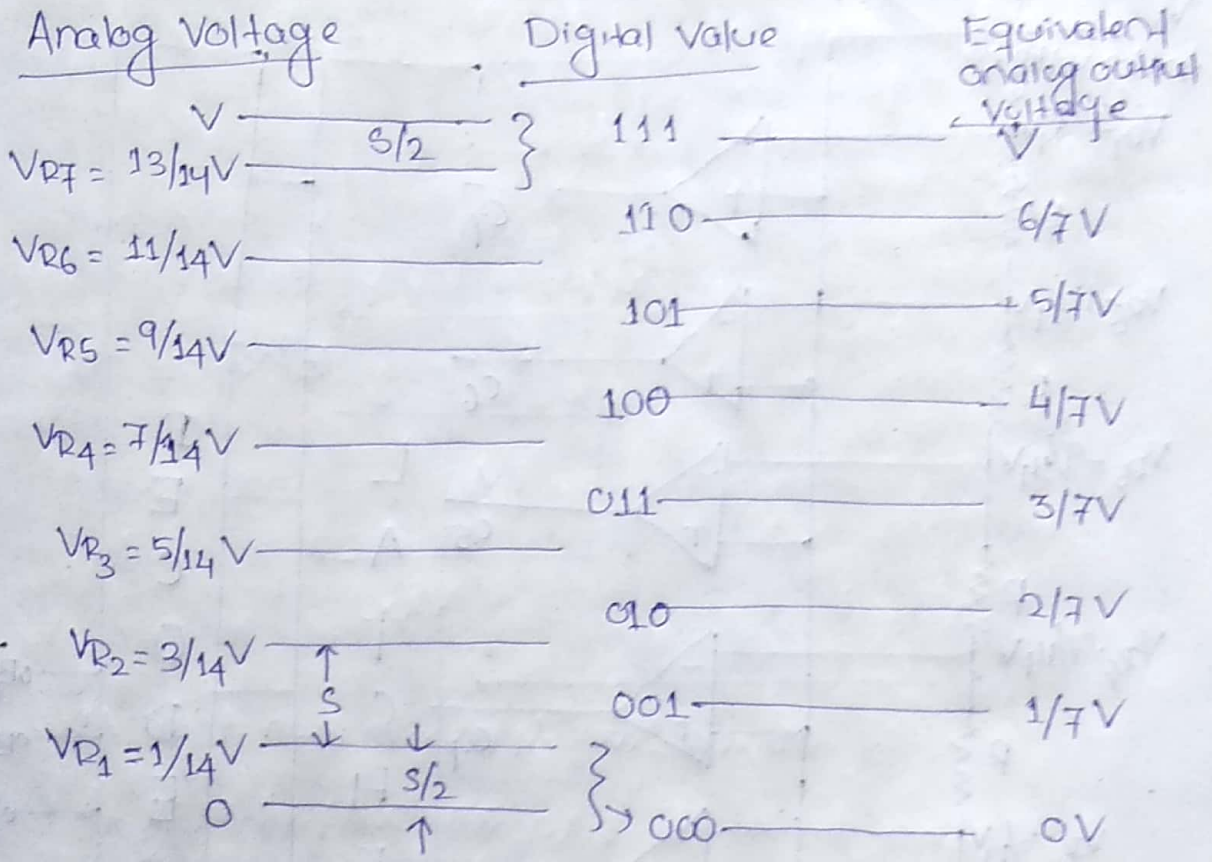
The intervals, along with their assigned digital values and equivalent analog output voltage if these digital signals are applied to a D/A converter are shown



This shows that the maximum quantization error will be $S/2 = V/14$ for any analog input voltage Va in the range 0 to V. The quantization error can also be specified in terms of LSB. For example, in the above case, the maximum quantization error is $\pm\frac{1}{2}$ LSB.

Parallel-comparator A/D converters

A 3 bit Parallel-comparator A/D converter is shown in Figure. Va is the analog voltage to be converted into digital form. The voltage corresponding to full scale is V from which the reference voltages $V_{R1}, V_{R2}, \ldots$ are generated using the resistor network.

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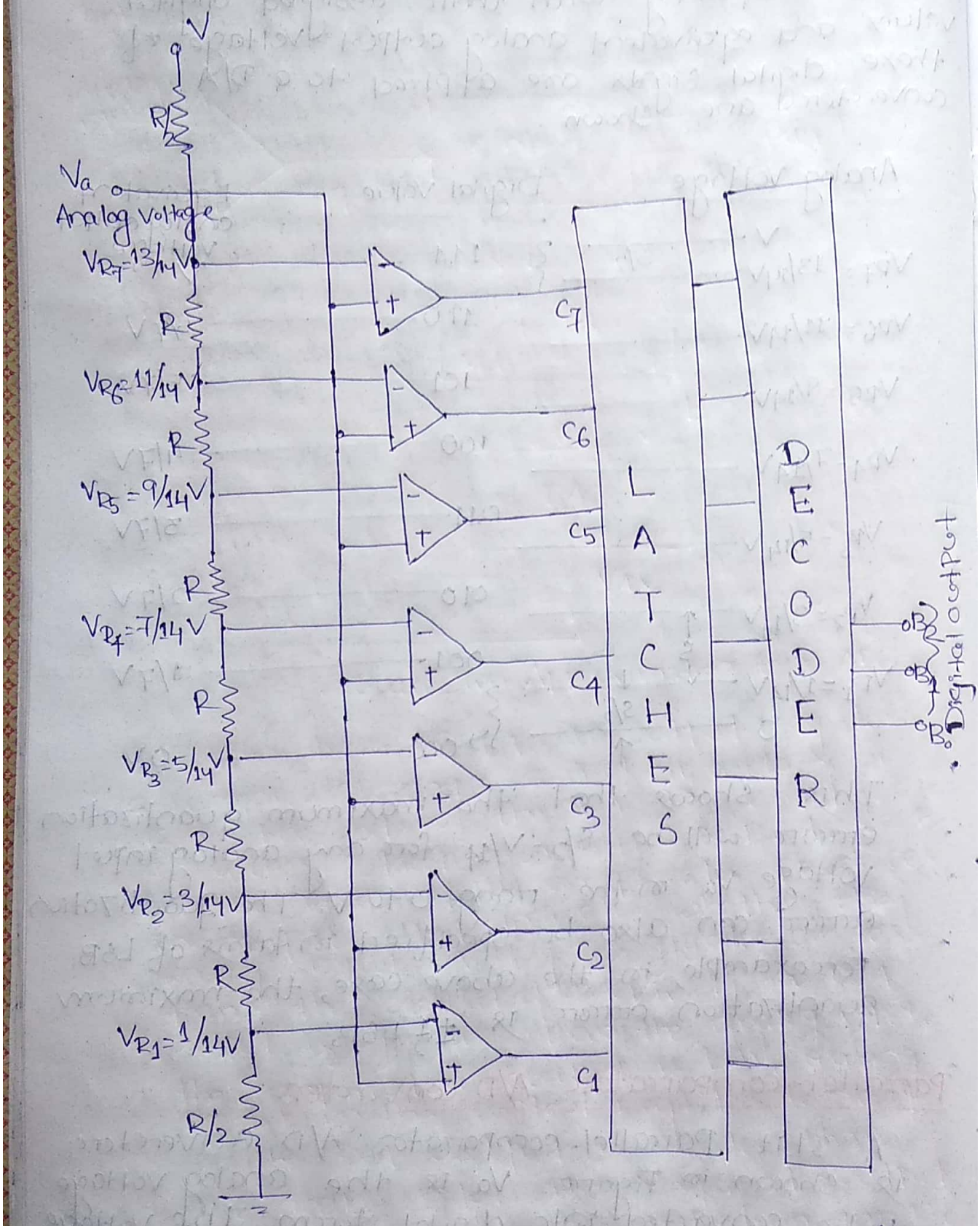

3 bit parallel comparator A/D converter

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the voltage Va is compared simultaneously with reference voltages by using comparators. A 7-bit output is obtained from the comparators which is stored in Latches. This 7-bit digital signal is converted to a 3-bit output by using a decoder circuit. The comparator outputs and the 3-bit digital output for each interval of the analog voltage are given in Table below

Analog input Va	Comparator outputs C7 C6 C5 C4 C3 C2 C1	Digital output B2 B1 B0
$0 \le V_a < V_{R1}$	0 0 0 0 0 0 0	0 0 0
$V_{R1} < V_a < V_{R2}$	0 0 0 0 0 0 1	0 0 1
$V_{R2} < V_a < V_{R3}$	0 0 0 0 0 1 1	0 1 0
$V_{R3} < V_a < V_{R4}$	0 0 0 0 1 1 1	0 1 1
$V_{R4} < V_a < V_{R5}$	0 0 0 1 1 1 1	1 0 0
$V_{R5} < V_a < V_{R6}$	0 0 1 1 1 1 1	1 0 1
$V_{R6} < V_a < V_{R7}$	0 1 1 1 1 1 1	1 1 0
$V_{R7} < V_a \le V$	1 1 1 1 1 1 1	1 1 1

The principle of parallel-comparator A/D conversion is the simplest in concept and fastest. Its main disadvantages are rapid increase in the number of comparators with the number of bits [$(2^N - 1)$ comparators are required for an N-bit comparator] and the corresponding complications of the decoder circuit.

Successive Approximation A/D converter

The successive-approximation A/D converter is one of the most widely used type of ADCs. It has a much shorter conversion time than the other types. It has also a fixed conversion time which is not dependent on the value of the analog input signal.

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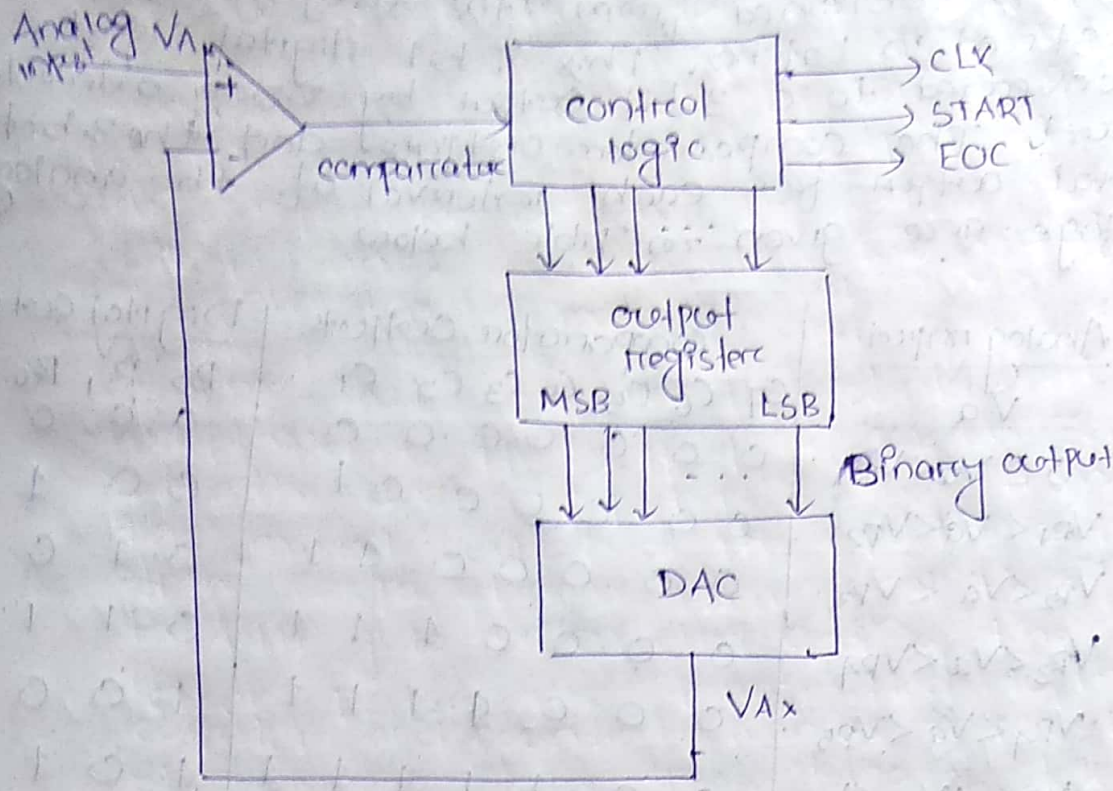

Successive-Approximation type ADC

It consists of a DAC, an output register, a comparator, and a control circuitary or logic. The bits of the DAC are enabled one at a time, starting with the MSB. As each bit is enabled, the comparator produces an output that indicates whether the analog input voltage is greater or less than the output of DAC V_{Ax}. If the D/A output is greater than the analog input, the comparator output is LOW, causing the bit in the control register to reset. If the D/A output is greater than the analog input, the comparator output is HIGH, and the bit is retained in the control register.

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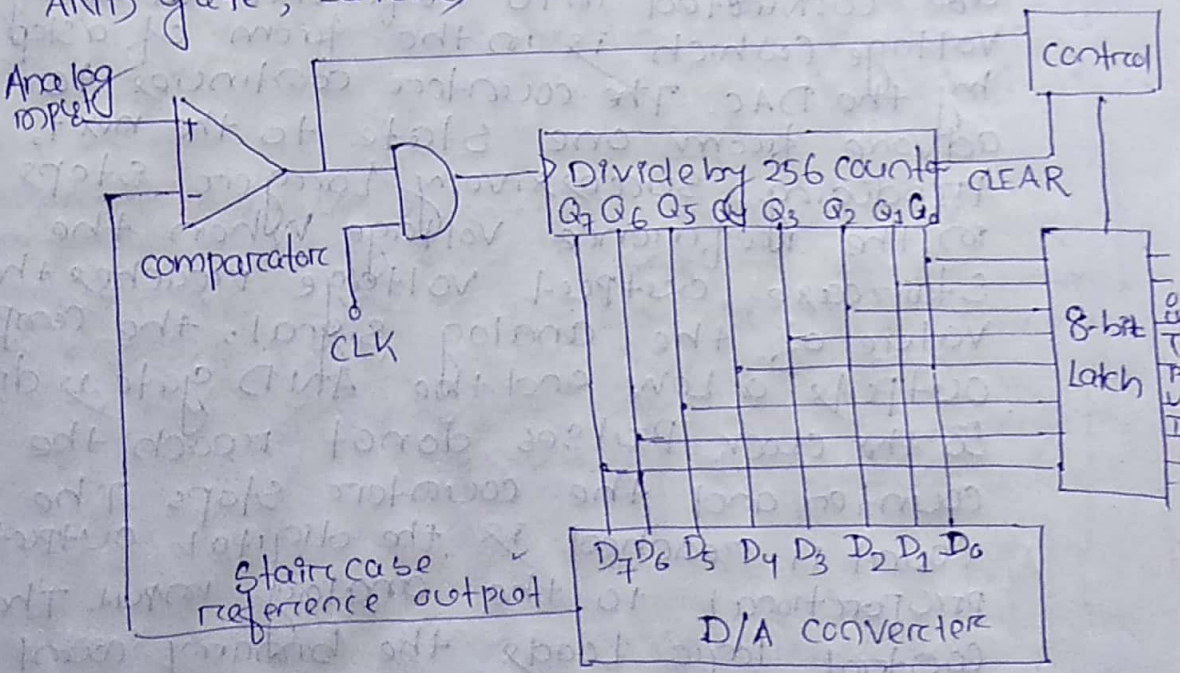
The system enables the MSB first, then the next significant bit, and so on. After all the bits of DAC have been tried, the conversion cycle is complete. The processing of each bit takes one clock cycle, so the total conversion time for an N-bit SA-type ADC will be N clock cycles. That is:

$$t_c \text{ for SAC} = (N \times 1) \text{ clock cycle}$$

The conversion time will be the same regardless of the value of VA. This is because the control logic has to process each bit to see whether a 1 is needed or not.

Counting A/D converter

This is the simplest type of A/D converter. It employs a binary counter, a voltage comparator, a control logic circuit, an AND gate, Latches and a D/A converter.



Logic diagram of the counter type ADC.

It is also called a digital ramp ADC, because the waveform at the output of DAC is a step-by-step ramp (actually a staircase). The analog signal to be converted is applied to the non-inverting terminal of the op-amp comparator. The output of the

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DAC is applied to the inverting terminal of the op-amp. Whenever the analog input signal is greater than the DAC output, the output of the op-amp is HIGH and whenever the output of the DAC is greater than the analog signal, the output of the comparator is LOW. The comparator output serves as an active-Low end of the conversion signal.

Assume that initially the counter is reset and therefore, the output of DAC is Zero. Since the analog input is Larger than the initial output of the DAC, the output of the comparator is HIGH and therefore, the AND gate is enabled and so, the clock pulses are transmitted to the counter and counter advances through its binary states. These binary states are converted into reference analog voltage (which is in the form of a step) by the DAC. The counter continues to advance from one state to the next, producing successively Larger steps in the reference voltage. When the staircase output voltage reaches the value of the analog signal, the comparator outputs a LOW and the AND gate is disabled, so the clock pulses do not reach the counter and the counter stops. The count it reached is the digital output proportional to the analog input. The control logic Loads the binary count in to the latches and resets the counter, thus beginning another count sequence to sample the input value. The cycle thus repeats itself.

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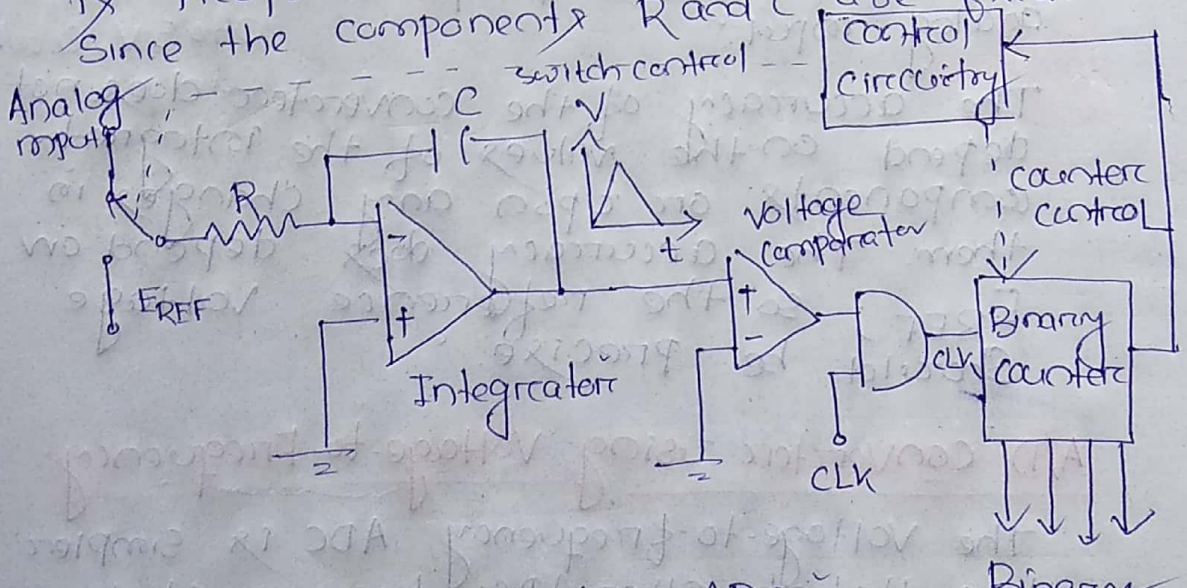
Dual-Slope Type A/D convereters

The dual-slope converters is one of the slowest converters, but is relatively inexpensive because it does not require precision components such as a DAC or VCO. Another advantage of the dual-slope ADC is its low sensitivity to noise and to variations in its component values caused by temperature changes. Because of the large conversion time, the dual-slope ADC is not used in any data acquisition applications. The major applications of this type of converter are in digital voltmeters, multimeters etc where slow conversion are not a problem. Since it is not fast enough, its use is restricted to signals having low to medium frequencies.

A dual-slope ADC uses an operational amplifier to integrate the analog input. The output of the integrator is a ramp, whose slope is proportional to the input signal Ein, Since the components R and C are fixed.



The dual-slope ADC

Assume that the input is a negative voltage and is constant for a period of time; so the output of the integrator is a positive ramp. The ramp is allowed to continue for a fixed time and the voltage it reaches in that time is directly dependent on the analog input. The fixed time is controlled by sensing the time when the counter

reaches a particular count. At that time, the counter is reset and the control circuitry causes the switch to be connected to a reference voltage E_{REF}, having a polarity opposite to that of the analog input; in this case a positive reference voltage. Therefore, the output of the integrator is a negative going ramp, beginning from the positive value it reached during the first integration. The AND gate is enabled and the counter starts counting. When the ramp reaches to 0V, the voltage comparator switches to LOW, inhibiting the clock pulses and the counter stops counting. The binary count is latched, thus completing the conversion. The count it contains at that time is proportional to the time required for the negative ramp to reach Zero, which is proportional to the positive voltage reached during the first integration which in turn is proportional to the analog input.

The accuracy of the converter does not depend on the values of the integrator components or upon any changes in them. The accuracy does depend on E_{REF}; so the reference voltage should be precise.

A/D Converter using Voltage-to-Frequency

The voltage-to-frequency ADC is simpler than that of other ADCs, because it does not use a DAC. Instead it uses a Linear Voltage controlled oscillator (VCO) that produces an output frequency proportional to its input voltage. The analog voltage is applied to the VCO to generate an output frequency. This frequency is fed to a counter, to be counted for

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a fixed time interval. The final count is proportional to the value of the analog input.

Although this is simple method of conversion, it is difficult to achieve a high degree of accuracy because of the difficulty in designing VCOs with accuracy better than 0.1 percent.

A/D Converter Using Voltage-to-time Conversion

In an A/D converter using voltage-to-frequency converter, the cycles of a variable frequency source are counted for a fixed period. Alternatively it is possible to make an A/D converter by counting the cycles of a fixed-frequency source for a variable period. For this, the analog voltage is required to be converted to a proportional time period.

Specifications of A/D Converters

The following specifications are usually specified by the manufacturers of A/D converters.

1. Range of input voltage
2. Input impedance
3. Accuracy
4. Conversion time
5. Format of digital output

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An Example of A/D Converter IC

The AD ADC 80 is a 12-bit successive approximation A/D converter available in a 32-pin DIP. Its important performance characteristics are

Linear error at +25°C	: ±0.012%
Maximum gain temperature coefficient	: 30 ppm/°C
Power dissipation	: 800 mW
Maximum conversion time	: 25 µs
Digital output format	: Unipolar & bipolar; parallel & serial
Output drive	: 2 TTL Loads
Analog voltage ranges	: ±2.5V, ±5V, ±10V (bipolar) or 0 to 5V, 0 to 10V (unipolar)

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